PATENT COOPERATION TREATY 980

From the INTERNATIONAL BUREAU

PCT

NOTIFICATION OF ELECTION

(PCT Rule 61.2)

To:

Commissioner
US Department of Commerce
United States Patent and Trademark Office, PCT
2011 South Clark Place Room
CP2/5C24
Arlington, VA 22202
ETATS-UNIS D'AMERIQUE

in its capacity as elected Office

Date of mailing (day/month/year)	
14 May 2001 (14.05.01)	
International application No.	**Applicant's or agent's file reference**
PCT/CA00/00996	08-887955WO
International filing date (day/month/year)	**Priority date** (day/month/year)
01 September 2000 (01.09.00)	01 September 1999 (01.09.99)
Applicant	
MANKU, Tajinder et al	

1. The designated Office is hereby notified of its election made:

   [X] in the demand filed with the International Preliminary Examining Authority on:

   29 March 2001 (29.03.01)

   [ ] in a notice effecting later election filed with the International Bureau on:

   _____

2. The election [X] was

   [ ] was not

   made before the expiration of 19 months from the priority date or, where Rule 32 applies, within the time limit under Rule 32.2(b).

The International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland

Facsimile No.: (41-22) 740.14.35

Authorized officer

Céline Faust

Telephone No.: (41-22) 338.83.38

PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:
WADA, Ikuku et al.
Gowling Lafleur Henderson LLP
Suite 2600
160 Elgin Street
Ottawa, Ontario K1P 1C3
CANADA

WRITTEN OPINION

(PCT Rule 66)

Date of mailing *(day/month/year)*	25/10/2002
Applicant's or agent's file reference: 08-891710WO	**REPLY DUE** within **2** / 00 months/days from the above date of mailing

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/CA 01/ 00876	19/06/2001	01/09/2000

International Patent Classification (IPC) or both national classification and IPC
H04B1/00

Applicant
SIRIFIC WIRELESS CORPORATION et al.

1. This written opinion is the first drawn up by this International Preliminary Examining Authority.
2. This opinion contains indications relating to the following items:
   - I [X] Basis of the opinion
   - II [ ] Priority
   - III [ ] Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV [ ] Lack of unity of invention
   - V [X] Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
   - VI [ ] Certain documents cited
   - VII [ ] Certain defects in the international application
   - VIII [ ] Certain observations on the international application
3. The applicant is hereby **invited to reply** to this opinion.
   - **When?** See the time limit indicated above. The applicant may, before the expiration of that time limit, request this Authority to grant an extension, see Rule 66.2(d).
   - **How?** By submitting a written reply, accompanied, where appropriate, by amendments, according to Rule 66.3. For the form and the language of the amendments, see Rules 66.8 and 66.9.
   - **Also** For an additional opportunity to submit amendments, see Rule 66.4. For the examiner's obligation to consider amendments and/or arguments, see Rule 66.4*bis*. For an informal communication with the examiner, see Rule 66.6.

   If no reply is filed, the international preliminary examination report will be established on the basis of this opinion.
4. The final date by which the international preliminary examination report must be established according to Rule 69.2 is: 01/01/2003

Name and mailing address of the IPEA/
European Patent Office
D-80298 Munich
Tel. (+49-89) 2399-0, Tx: 523656 epmu d
Fax: (+49-89) 2399-4465

Authorized officer
Examiner

Formalities officer
(incl. extension of time limits)
Tel. (+49-89) 2399 2828

EUROPÄISCHES PATENTAMT · EUROPEAN PATENT OFFICE · OFFICE EUROPÉEN DES BREVETS

I. Basis of the opinion

1. The basis of this written opinion is the application as originally filed.

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability

1. In light of the documents cited in the international search report, it is considered that the invention as defined in at least some of the claims does not appear to meet the criteria mentioned in Article 33(1) PCT, i.e. does not appear to be novel and/or to involve an inventive step (see international search report, in particular the documents cited X and/or Y and corresponding claims references).

2. If amendments are filed, the applicant should comply with the requirements of Rule 66.8 PCT and indicate the basis of the amendments in the documents of the application as originally filed (Article 34 (2) (b) PCT) otherwise these amendments may not be taken into consideration for the establishment of the international preliminary examination report. The attention of the applicant is drawn to the fact that if the application contains an unnecessary plurality of independent claims, no examination of any of the claims will be carried out.

NB: Should the applicant decide to request detailed substantive examination, then an international preliminary examination report will normally be established directly. Exceptionally the examiner may draw up a second written opinion, should this be explicitly requested.

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
8 March 2001 (08.03.2001)

PCT

(10) International Publication Number
WO 01/17122 A1

(51) International Patent Classification[7]: H04B 1/26, 1/28, H03D 7/16

(21) International Application Number: PCT/CA00/00996

(22) International Filing Date:
1 September 2000 (01.09.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
2,281,236 1 September 1999 (01.09.1999) CA

(71) Applicant *(for all designated States except US)*: SiRiFIC WIRELESS CORPORATION [CA/CA]; 1 Bluespring Drive, Unit 302, Waterloo, Ontario N2J 4M1 (CA).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: MANKU, Tajinder [CA/CA]; 4 Jacqueline Place, Kitchener, Ontario N2N 3K9 (CA). SNYDER, Chris [CA/CA]; RR#1 Pleasantville, Lunenburg County, Nova Scotia B0R 1G0 (CA). WEALE, Gareth [CA/CA]; 61 Waterloo Street, New Hamburg, Ontario N0B 2G0 (CA). WONG, Lawrence [CA/CA]; 50 Waterbridge Lane, Markham, Ontario L3R 8V9 (CA).

(74) Agents: HARRIS, John, D. et al.; Gowling Lafleur Henderson LLP, 160 Elgin Street, Suite 2600, Ottawa, Ontario K1P 1C3 (CA).

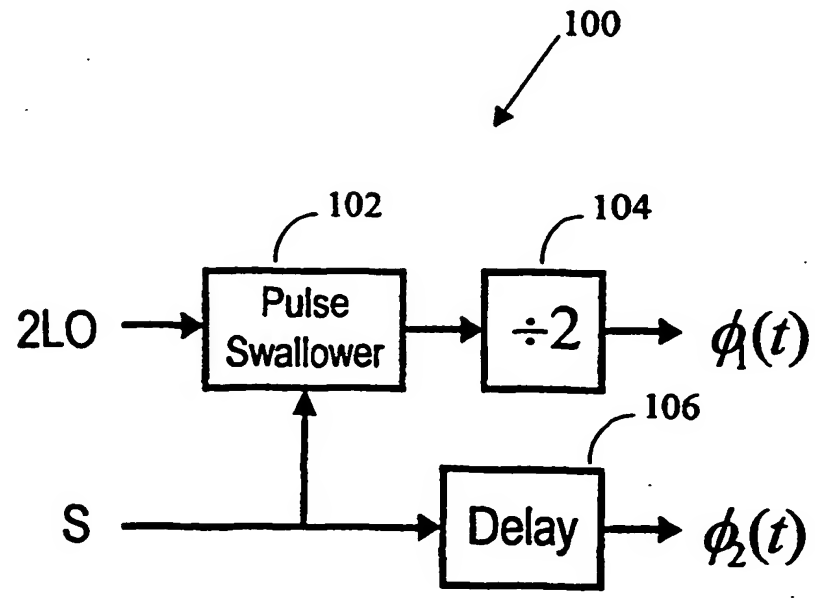
(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *With international search report.*
— *Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: IMPROVED METHOD AND APPARATUS FOR UP- AND DOWN-CONVERSION OF RADIO FREQUENCY (RF) SIGNALS



(57) Abstract: This patent describes a method and system which overcomes the LO-leakage problem of direct conversion and similar RF transmitters and receivers. To solve this problem a virtual LO™ signal is generated which emulates mixing with a local oscillator (LO) signal. However, the virtual local oscillator (VLO) signal is constructed using signals that do not contain a significant amount of power (or no power at all) at the wanted output RF frequency, so there is no LO component to leak to the output. The invention also does not require sophisticated filters or large capacitors as other designs in the art, so it is fully integratable.

WO 01/17122 A1

Improved Method and Apparatus for Up- and Down- Conversion of Radio Frequency (RF) Signals

The present invention relates generally to communications, and more specifically, to a fully-integrable method and apparatus for up- and down-conversion of radio frequency (RF) and baseband signals with improved performance.

Background of the Invention

Many communication systems modulate electromagnetic signals from baseband to higher frequencies for transmission, and subsequently demodulate those high frequencies back to their original frequency band when they reach the receiver. The original (or baseband) signal, may be, for example: data, voice or video. These baseband signals may be produced by transducers such as microphones or video cameras, be computer generated, or transferred from an electronic storage device. In general, the high transmission frequencies provide longer range and higher capacity channels than baseband signals, and because high frequency RF signals can propagate through the air, they can be used for wireless channels as well as hard wired or fibre channels.

All of these signals are generally referred to as radio frequency (RF) signals, which are electromagnetic signals, that is, waveforms with electrical and magnetic properties within the electromagnetic spectrum normally associated with radio wave propagation. The electromagnetic spectrum was traditionally divided into 26 alphabetically designated bands, however, the International Telecommunication Union (ITU) formally recognizes 12 bands, from 30 Hz to 3000 GHz. New bands, from 3 THz to 3000 THz, are under active consideration for recognition.

Wired communication systems which employ such modulation and demodulation techniques include computer communication systems such as local area networks (LANs), point to point signalling, and wide area networks (WANs) such as the Internet. These networks generally communication data signals over electrical or optical fibre channels. Wireless communication systems which may employ modulation and demodulation include those for public broadcasting such as AM and FM radio, and UHF and VHF television. Private communication systems may include cellular telephone networks, personal paging devices, HF radio systems used by taxi services, microwave backbone networks, interconnected appliances under the Bluetooth standard, and satellite communications. Other wired and

wireless systems which use RF modulation and demodulation would be known to those skilled in the art.

One of the current problems in the art, is to develop physically small and inexpensive modulation and demodulation techniques and devices that have good performance characteristics. For cellular telephones, for example, it is desirable to have transmitters and receivers (which may be referred to in combination as a transceiver) which can be fully integrated onto integrated circuits (ICs).

Several attempts at completely integrated transceiver designs have met with limited success. For example, most RF topology typically requires at least two high quality filters that cannot be economically integrated within any modern IC technology. Other RF receiver topologies exist, such as image rejection architectures, which can be completely integrated on a chip, but lack in overall performance. Most receivers use the "super-heterodyne" topology, which provides excellent performance, but does not meet the desired level of integration for modern wireless systems.

Existing transceiver solutions and their associated problems and limitations are summarized below.

1. Super-heterodyne:

The super-heterodyne receiver uses a two-step frequency translation method to convert an RF signal to a baseband signal. **Figure 1** presents a block diagram of a typical super-heterodyne receiver **10**. Generally, the mixers labelled M1 **12**, MI **14**, and MQ **16** are used to translate an incoming RF signal to baseband or to some intermediate frequency (IF). The balance of the components amplify the signal being processed and filter noise from it.

More specifically, the RF band pass filter (BPF1) **18** first filters the incoming signal and corruptive noise coming from the antenna **20**, attenuating out of band signals and passing the desired signal (note that this band pass filter **18** may also be a duplexer). A low noise amplifier **22** then amplifies the filtered antenna signal, increasing the strength of the RF signal and reducing the noise figure of the receiver **10**. The signal is next filtered by another band pass filter (BPF2) **24** usually identified as an image rejection filter. The desired signal, plus residual unwanted signals, then enter mixer M1 **12** which multiplies this signal with a periodic sinusoidal signal generated by the local oscillator (LO1) **26**. The mixer M1 **12** receives the signal from the image rejection filter **24** and causes both a down-conversion and an up-

conversion in the frequency domain. Usually, the down-converted portion is retained at the so-called "Intermediate Frequency" (IF).

Generally, a mixer is a circuit or device that accepts as its input two different frequencies and presents at its output:

(a) a signal equal in frequency to the sum of the frequencies of the input signals;

(b) a signal equal in frequency to the difference between the frequencies of the input signals; and

(c) the original input frequencies.

Note that the frequency conversion process causes a second band of frequencies to be superimposed upon the desired signal at the IF frequency. These "image frequencies" are also passed by the band pass filter **24** and corrupt the desired signal. Note also that the typical embodiment of a mixer is a digital switch, which may generate significantly more tones than those described in (a) through (c).

The IF signal is next filtered by a band pass filter (BPF3) **28** typically called the channel filter, which is centred around the IF frequency, thus filtering out mixer signals (a) and (c) above.

The signal is then amplified by an amplifier (IFA) **30**, and is split into its in-phase (I) and quadrature (Q) components, using mixers MI **14** and MQ **16**, and orthogonal mixing signals generated by local oscillator (LO2) **32** and 90 degree phase shifter **34**. LO2 **32** generates a regular, periodic signal which is typically tuned to the IF frequency, so that the signals coming from the outputs of MI **14** and MQ **16** are now at baseband, that is, the frequency at which they were originally generated. The two signals are next filtered using low pass filters LPFI **36** and LPFQ **38** to remove the unwanted products of the mixing process, producing baseband I and Q signals. The signals may then be amplified by gain-controlled amplifiers AGCI **40** and AGCQ **42**, and digitized via analog to digital converters ADI **44** and ADQ **46** if required by the receiver.

The main problems with the super-heterodyne design are:

- it requires expensive off-chip components, particularly band pass filters **18**, **24**, **28**, and low pass filters **36**, **38** to remove unwanted signal components;
- the off-chip components require design trade-offs that increase power consumption and reduce system gain;
- image rejection is limited by the off-chip components, not by the target integration technology;
- isolation from digital noise can be a problem; and

- it is not fully integratable.

2. Image Rejection Architectures:

Several image rejection architectures exist, but are not widely used. The two most well known being the Hartley Image Rejection Architecture and the Weaver Image Rejection Architecture. There are other designs, which are generally based on these two architectures, and other methods which employ poly-phase filters to cancel image components. Generally, either accurate signal phase shifts or accurate generation of quadrature local oscillators are employed in these architectures to cancel the image frequencies. The amount of image cancellation is directly dependent upon the degree of accuracy in producing the phase shift or in producing the quadrature local oscillator signals.

Although the integratability of these architectures is high, their performance is relatively poor due to the required accuracy of the phase shifts and quadrature oscillators. This architecture has been used for dual mode receivers on a single chip.

3. Direct Conversion:

Direct conversion architectures demodulate RF signals to baseband in a single step, by mixing the RF signal with a local oscillator signal at the carrier frequency of the RF signal. There is therefore no image frequency, and no image components to corrupt the signal. Direct conversion receivers offer a high level of integratability, but also have several important problems. Hence, direct conversion receivers have thus far proved useful only for signalling formats that do not place appreciable signal energy near DC after conversion to baseband.

A typical direct conversion receiver is shown in **Figure 2**. The RF band pass filter (BPF1) **18** first filters the signal coming from the antenna **20** (this band pass filter **18** may also be a duplexer). A low noise amplifier **22** is then used to amplify the filtered antenna signal, increasing the strength of the RF signal and reducing the noise figure of the receiver **10**.

The signal is then split into its quadrature components and demodulated in a single stage using mixers MI **14** and MQ **16**, and orthogonal signals generated by local oscillator (LO2) **32** and 90 degree phase shifter **34**. LO2 **32** generates a regular, periodic signal which is tuned to the incoming wanted frequency rather than an IF frequency as in the case of the super-heterodyne receiver. The signals coming from the outputs of MI **14** and MQ **16** are now at baseband, that is, the frequency at which they were originally generated. The two signals are next filtered

using low pass filters LPFI **36** and LPFQ **38**, are amplified by gain-controlled amplifiers AGCI **40** and AGCQ **42**, and are digitized via analog to digital converters ADI **44** and ADQ **46**.

Direct conversion RF receivers have several advantages over super-heterodyne systems in term of cost, power, and level of integration, however, there are also several serious problems with direct conversion. These problems include:

- noise near baseband (that is, 1/f noise) which corrupts the desired signal;
- local oscillator (LO) leakage in the RF path that creates DC offsets. As the LO frequency is the same as the incoming signal being demodulated, any leakage of the LO signal onto the antenna side of the mixer will pass through to the output side as well;
- local oscillator leakage into the RF path that causes desensitization. Desensitation is the reduction of desired signal gain as a result of receiver reaction to an undesired signal. The gain reduction is generally due to overload of some portion of the receiver, such as the AGC circuitry, resulting in suppression of the desired signal because the receiver will no longer respond linearly to incremental changes in input voltage.
- noise inherent to mixed-signal integrated circuits corrupts the desired signal;
- large on-chip capacitors are required to remove unwanted noise and signal energy near DC, which makes integrability expensive. These capacitors are typically placed between the mixers and the low pass filters; and
- errors are generated in the quadrature signals due to inaccuracies in the 90 degree phase shifter.

4. Near Zero-IF Conversion:

This receiver architecture is similar to the direct conversion architecture, in that the RF input signal band is translated brought close to baseband in a single step using a regular, periodic oscillator signal. However, the desired signal is not brought exactly to baseband and therefore DC offsets and 1/f noise do not contaminate the output signal. Image frequencies are again a problem though, as in the case of the super-heterodyne structure.

Additional problems encountered with near zero-IF architectures include:

- the need for very accurate quadrature local oscillators;
- the need for several balanced signal paths for purposes of image cancellation;

- noise inherent to mixed-signal integrated circuits which corrupts the desired output signal; and
- isolation from digital noise can be a problem.

5. Sub-sampling Down-conversion:

This method of signal down-conversion utilizes subsampling of the input signal to effect the frequency translation, that is, the input signal is sampled at a lower rate than the signal frequency. This may be done, for example, by use of a sample and hold circuit.

Although the level of integration possible with this technique is the highest among those discussed thus far, the subsampling down-conversion method suffers from two major drawbacks:

- subsampling of the RF signal causes aliasing of unwanted noise power to DC. Sampling by a factor of m increases the down-converted noise power of the sampling circuit by a factor of $2m$; and
- subsampling also increases the effect of noise in the sampling clock. In fact, the clock phase noise power is increased by m^2 for sampling by a factor of m.

There is therefore a need for a method and apparatus of modulating and demodulating RF signals which allows the desired integrability along with good performance.

Summary of the Invention

It is therefore an object of the invention to provide a novel method and system of modulation and demodulation which obviates or mitigates at least one of the disadvantages of the prior art.

One aspect of the invention is broadly defined as a first signal generator for producing a first time-varying signal φ_1; and a second signal generator for producing a second time-varying signal φ_2; where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of the local oscillator signal being emulated.

Brief Description of the Drawings

These and other features of the invention will become more apparent from the following description in which reference is made to the appended drawings in which:

Figure 1 presents a block diagram of a super-heterodyne system as known in the art;

Figure 2 presents a block diagram of a direct conversion transmitter as known in the art;

Figure 3 presents a mixer and synthesizer arrangement in a broad embodiment of the invention;

Figure 4 (a) presents a first exemplary mixer input signals pairing plotted in amplitude against time, in an embodiment of the invention;

Figure 4 (b) presents a second exemplary mixer input signals pairing plotted in amplitude against time, in an embodiment of the invention;

Figure 5 presents a mixer and synthesizer arrangement for modulation or demodulation of in-phase and quadrature components of an input signal in an embodiment of the invention;

Figure 6 presents a block diagram of an exemplary signal synthesizer in an embodiment of the invention, employing a pulse swallower and a divide-by-2 circuit;

Figure 7 presents a logic diagram of an exemplary signal synthesizer for generating quadrature mixer signals, in an embodiment of the invention;

Figure 8 presents a logic diagram of an exemplary signal synthesizer in an embodiment of the invention, employing a shift register;

Figure 9 presents a logic diagram of an exemplary signal synthesizer in an embodiment of the invention, employing two shift registers;

Figure 10 presents a logic diagram of an exemplary signal synthesizer in an embodiment of the invention, employing an input signal with a frequency equal to the RF carrier;

Figure 11 presents a logic diagram of an exemplary signal synthesizer in an embodiment of the invention, employing a shift register with feedback; and

Figure 12 presents a block diagram of an embodiment of the invention employing N mixers and N time-domain signals.

Detailed Description of the Invention

The present invention relates to the frequency translation of RF signals to and from baseband in highly integrated receivers and transmitters. It is particularly concerned with the generation of signals used in the translation process which have properties that solve the image-rejection problems associated with heterodyne receivers and transmitters and the LO-leakage and 1/f noise problems associated with direct conversion receivers and transmitters.

A circuit which addresses the objects outlined above, is presented as a block diagram in **Figure 3**. This figure presents a modulator or demodulator topography **70** in which an input signal *x(t)* is mixed with two synthesized signals (labelled φ_1 and φ_2) which are irregular and vary in the time domain (TD), to effect the desired modulation or demodulation. The two mixers M1 **72** and M2 **74** are standard mixers known in the art, having the typical properties of an associated noise figure, linearity response, and conversion gain. The selection and design of these mixers would follow the standards known in the art, and could be, for example, double balanced mixers. Though this figure implies various elements are implemented in analogue form they can be implemented in digital form.

The two synthesizers **76** and **78** generate two time-varying functions φ_1 and φ_2 that together comprise a virtual local oscillator (VLO) signal. These two functions have the properties that their product emulates a local oscillator (LO) signal that has significant power at the carrier frequency, but neither of the two signals has a significant level of power at the frequency of the LO being emulated. As a result, the desired modulation or demodulation is affected, but there is no LO signal to leak into the RF path.

The representation in **Figure 3** is exemplary, as any two-stage or multiple stage mixing architecture may be used to implement the invention. As well, the synthesizer for generating the time-varying mixer signals φ_1 and φ_2 may be comprised of a single device, or multiple devices.

In current receiver and transmitter technology, frequency translation of an RF signal to and from baseband is performed by multiplying the input signal by regular, periodic, sinusoids. If one multiplication is performed, the architecture is said to be a direct-conversion or homodyne architecture, while if more than one multiplication is performed the architecture is said to be a heterodyne or super-heterodyne architecture. Direct-conversion transceivers suffer from LO leakage and 1/f noise

problems which limit their capabilities, while heterodyne transceivers require image-rejection techniques which are difficult to implement on-chip with high levels of performance.

The problems of image-rejection, LO leakage and 1/f noise in highly integrated transceivers can be overcome by using more complex signals than simple, regular, periodic, sinusoids in the frequency translation process. These signals have tolerable amounts of power at the RF band frequencies both in the signals themselves and in any other signals produced during their generation. Two example of such signals (φ_1 and φ_2) are presented in **Figures 4(a)** and **4(b)**, and are described in detail hereinafter.

The preferred criteria for selecting the functions φ_1 and φ_2 are:

(i) for the signal *x(t)* to be translated to baseband, $\varphi_1(t) * \varphi_2(t)$ must have a frequency component at the carrier frequency of *x(t)*;

(ii) in order to minimize image problems, $\varphi_1(t) * \varphi_2(t)$ must have less than a tolerable amount energy at frequencies other than the carrier frequency of x(t) or at least far enough away that these image frequencies can be significantly filtered on-chip prior to down-conversion; and

(iii) in order to minimize LO leakage problems, the signals φ_1 and φ_2 must not have significant amounts of power in the RF output signal bandwidth. That is, the amount of power generated at the output frequency should not effect the overall system performance of the transmitter or receiver in a significant manner;

(iv) also to avoid LO leakage found in conventional direct conversion and directly modulated topologies, the signals required to generate φ_1 and φ_2 or the intermediate signals which occur, should not have a significant amount of power at the output frequency;

(v) $\varphi_2 * \varphi_2$ should not have a significant amount of power within the bandwidth of the up-converted RF (output) signal. This ensures that if φ_1 leaks into the input port, it does not produce a signal within the RF signal at the output. It also ensures that if φ_2 leaks into node between the two mixers, it does not produce a signal within the RF signal at the output; and

(vi) if *x(t)* is an RF signal, $\varphi_1 * \varphi_1 * \varphi_2$ should not have a significant amount of power within the bandwidth of the RF signal at baseband. This ensures that if φ_1 leaks into the input port, it does not produce a signal within the baseband signal at the output.

These signals can, in general, be random, pseudo-random, periodic functions of time, analogue or digital waveforms.

It would be clear to one skilled in the art that virtual LO signals may be generated which provide the benefits of the invention to greater or lesser degrees. While it is possible in certain circumstances to have almost no LO leakage, it may be acceptable in other circumstances to incorporate virtual LO signals which still allow a degree of LO leakage.

Exemplary sets of acceptable waveforms are presented in **Figures 4(a)** and **4(b)**, plotted in amplitude versus time. In **Figure 4(a)**, five cycles of the VLO signal are presented, labelled φ_1 φ_2. It is important to note that at no point in the operation of the circuit is an actual "φ_1 φ_2" signal ever generated; the mixers receive separate φ_1 and φ_2 signals, and mix them with the input signal using different physical components. Hence, there is no LO signal which may leak into the circuit. The states of these φ_1 and φ_2 signals with respect to the hypothetical φ_1 φ_2 output are as follows:

φ_1 φ_2	φ_1	φ_2
Cycle 1 - LO	HI	LO
Cycle 1 - HI	LO	LO
Cycle 2 - LO	HI	LO
Cycle 2 - HI	LO	LO
Cycle 3 - LO	LO	HI
Cycle 3 - HI	LO	LO
Cycle 4 - LO	HI	LO
Cycle 4 - HI	LO	LO
Cycle 5 - LO	LO	HI
Cycle 5 - HI	HI	HI

Similarly, **Figure 4(b)** presents a second exemplary set of acceptable waveforms, plotted in amplitude versus time. In this case, however, the waveforms

repeat on a four cycle pattern. The states of these φ_1 and φ_2 signals with respect to the hypothetical φ_1 φ_2 output are as follows:

φ_1 φ_2	φ_1	φ_2
Cycle 1 - LO	LO	LO
Cycle 1 - HI	HI	LO
Cycle 2 - LO	LO	LO
Cycle 2 - HI	HI	LO
Cycle 3 - LO	HI	HI
Cycle 3 - HI	LO	HI
Cycle 4 - LO	HI	HI
Cycle 4 - HI	LO	HI

While these signals may be described as "aperiodic", groups of cycles may be repeated successively. For example, the pattern of the φ_1 and φ_2 input signals presented in **Figure 4(a)** which generate the $\varphi_1 * \varphi_2$ signal, repeat with every five cycles. Similarly, the pattern of the φ_1 and φ_2 input signals presented in **Figure 4(b)** repeat with every four cycles. Longer cycles could certainly be used.

It would be clear to one skilled in the art that many additional pairings of signals may also be generated. The more thoroughly the above criteria (i) - (vi) for selection of the φ_1 and φ_2 signals are complied with, the more effective the invention will be in overcoming the problems in the art.

As well, rather than employing two mixing signals shown above, sets of three or more may be used (additional description of this is given hereinafter with respect to **Figure 12**).

The topology of the invention is similar to that of two stage or multistage modulators and demodulators, but the use of irregular, time-varying mixer signal provides fundamental advantages over known transmitters and receivers. For example:

- minimal 1/f noise;
- minimal imaging problems;
- minimal leakage of a local oscillator (LO) signal into the RF output band;
- removes the necessity of having a second LO and various (often external) filters; and

- has a higher level of integration as the components it does require are easily placed on an integrated circuit. For example, no large capacitors or sophisticated filters are required.

The invention provides the basis for fully integrated communications transmitters and receivers. Increasing levels of integration have been the driving impetus towards lower cost, higher volume, higher reliability and lower power consumer electronics since the inception of the integrated circuit. This invention will enable communications devices to follow the same integration route that other consumer electronic products have benefited from.

Specifically, advantages from the perspective of the manufacturer when incorporating the invention into a product include:

1. significant cost savings due to the decreased parts count of an integral device. Decreasing the parts count reduces the cost of inventory control, reduces the costs associated with warehousing components, and reduces the amount of manpower to deal with higher part counts;
2. significant cost savings due to the decreased manufacturing complexity. Reducing the complexity reduces time to market, cost of equipment to manufacture the product, cost of testing and correcting defects, and reduces time delays due to errors and problems on the assembly line;
3. reduces design costs due to the simplified architecture. The simplified architecture will shorten the first-pass design time and total design cycle time as a simplified design will reduce the number of design iterations required;
4. significant space savings and increased manufacturability due to the high integrability and resulting reduction in product form factor (physical size). This implies huge savings throughout the manufacturing process as smaller device footprints enable manufacturing of products with less material such as printed circuit substrate, smaller product casing, and smaller final product packaging;
5. simplification and integrability of the invention will yield products with higher reliability, greater yield, less complexity, higher life span and greater robustness; and
6. due to the aforementioned cost savings, the invention will enable the creation of products that would otherwise be economically unfeasible.

Hence, the invention provides the manufacturer with a significant competitive advantage.

From the perspective of the consumer, the marketable advantages of the invention include:

- lower cost products, due to the lower cost of manufacturing;
- higher reliability as higher integration levels and lower parts counts imply products will be less prone to damage from shock, vibration and mechanical stress;
- higher integration levels and lower parts counts imply longer product life span;
- lower power requirements and therefore lower operating costs;
- higher integration levels and lower parts counts imply lighter weight and physically smaller products; and
- the creation of economical new products.

The invention can be applied in many ways which would be clear to one skilled in the art. A number of manners of creating VLO signals and applying them are described hereinafter, but it is understood that these embodiments are exemplary and not limiting.

Since the mixers in most transceivers act as solid state switches being turning on and off, it is preferable to drive the mixers using square waveforms rather than sinusoids. Square waveforms with steep leading and trailing edges will switch the state of the mixers more quickly, and at a more precise moment in time than sinusoid waveforms.

It is also important to note that in many modulation schemes, it is necessary to modulate or demodulate both in-phase (I) and quadrature (Q) components of the input signal, which requires a modulator or demodulator **90** as presented in the block diagram of **Figure 5**. In this case, four modulation functions would have to be generated: φ_{1I} which is 90 degrees out of phase with φ_{1Q}; and φ_{2I} which is 90 degrees out of phase with φ_{2Q}. The pairing of signals φ_{1I} and φ_{2I} must meet the function selection criteria listed above, as must the signal pairing of φ_{1Q} and φ_{2Q}. The mixers **92**, **94**, **96**, **98** are standard mixers as known in the art.

As shown in **Figure 5**, mixer M1I **92** receives the input signal *x(t)* and mixes it with φ_{1I}; subsequent to this, mixer M2I **94** mixes signal *x(t)* φ_{1I} with φ_{2I} to yield the in-phase component of the input signal, that is, *x(t)* $\varphi_{1I}\varphi_{2I}$. A complementary process occurs on the quadrature side of the demodulator, where mixer M1Q **96** receives the input signal *x(t)* and mixes it with φ_{1Q}; after which mixer M2Q **98** mixes signal *x(t)* φ_{1Q} with φ_{2Q} to yield the quadrature phase component of the input signal, that is, *x(t)* φ_{1Q}

φ_{2Q}. Several of the synthesizer **76**, **78** designs presented herein produce in-phase components only, but it would be clear to one skilled in the art how to generate complementary quadrature mixing signal pairs. Generally, separate in-phase and quadrature channels have not been identified in the interests of simplicity.

Several methods of generating such VLO signals are presented in **Figures 6** through **10**. Since the LO-leakage problem can occur when power is generated at frequencies in the RF band anywhere on chip, it is preferable that condition (iv) stated above be followed for intermediate signals produced during the generation of the signals φ_1 and φ_2. However, since the leakage path to these intermediate signals often provide some isolation, in such a case the condition on the intermediate signals can be somewhat relaxed.

The synthesizer **100** presented in **Figure 6** uses an input square wave (2LO) at twice the frequency of the RF carrier of the signal being modified by a signal denoted as *S*. Signal *S* could be the signal being modified, provided the criteria for the φ_1 and φ_2 signals are met, though generally it will be an independently generated control signal. This control signal *S* could also be generated using a delta-sigma (Δ - S) modulator which is known in the art.

A pulse swallower **102** is then used to remove pulses from the 2LO square wave. The pulse swallower **102** is controlled by the input signal *S*, such that when the input signal, *S*, switches state, a pulse is removed from the 2LO signal. The resulting signal is then passed through a divide-by-2 circuit **104** to produce the $\varphi_1(t)$ output signal. The input signal *S* passes through a delay circuit **106** which delays it by the amount of time it takes the 2LO signal to propagate through to the $\varphi_1(t)$ output, so that the two signals are synchronized. The output of this delay circuit **106** is the $\varphi_2(t)$ mixer signal.

Assuming that the input signal *S* follows no regular pattern, the output signals $\varphi_1(t)$ and $\varphi_2(t)$ could be random or pseudo-random. Since this circuit uses an oscillator at twice the carrier frequency of the input signal, there is no LO signal to leak to the output or into other parts of the circuit. Similarly, none of the intermediate signals, nor either of the mixer signals φ_1 and φ_2, has an LO frequency component.

A logic circuit that performs the function of **Figure 6** is presented in **Figure 7**. The pulse swallower **102** consists of a standard delay latch (D-latch) **D1**. A D-latch is a flip-flop whose input passes to the output after one clock cycle. The triggering of the pulse swallower **102** is controlled by D-latches **D4** through **D7** and the exclusive OR (XOR) gate **XOR1**, which detect the leading edge of the input signal *S* and

create a pulse which causes **D1** to swallow a pulse of the input signal 2LO. D-latches **D2** and **D3** form a divide-by-two circuit **104** that receives the output of **D1** and produces the φ_1 mixing signal. The D-latches **D4** through **D7** also delay the *S* signal to produce the φ_2 signal. Note that this circuit produces both the I and Q components of φ_1 and φ_2, which would be required for input to a mixer such as that of **Figure 5**; subscripts indicate the signals required for the frequency translation of the in-phase and quadrature components of the input signal *S*, respectively.

Figure 8 presents another method for producing the signals φ_1 and φ_2. Here, the D-latches **D8** through **D13** form a shift register which is clocked by the signal 2LO. The signal 2LO is once again a square wave that has a frequency of twice the RF carrier frequency. The shift register can be initially loaded with a predetermined sequence and the output φ_1 will cycle through that sequence producing the desired output. The second output φ_2 is then produced by taking the output of consecutive taps from the shift register, and exclusive-ORing them together with gate **XOR2** to produce a signal that can be used to clock a second shift register (**D14** and **D15**). The output of the second shift register is then φ_2.

Figure 9 shows a method similar to that of **Figure 8**, except that signal φ_2 is generated by a second shift register (**D22** through **D27**), which is a duplicate of the shift register that produces the signal φ_1 (**D16** through **D21**). As well, there is a difference in the initial loading of the shift registers; the first shift register being loaded with the sequence that will produce φ_1, and the second being loaded with the sequence which will produce φ_2.

The previous methods of generating φ_1 and φ_2 use an input signal at twice the RF carrier frequency (that is, 2LO). In some situations it may be difficult to design logic to operate at this frequency. If enough isolation can be obtained to protect an input of LO from leaking into the RF band, the method shown in **Figure 10** can be used.

Here the edges of the input signal *S* are aligned with the LO input edges through the D flip-flop **D28**. The inverter **I1** adds a delay to the LO input to make sure the two signal edges remain aligned. The two signals are then passed through an exclusive OR (XOR) gate **XOR3** to produce the output signal φ_1. Another delay is added to the output of the **D28** latch via invertor **I2** to keep the edges aligned with the output of the XOR gate **XOR3**. The output of **I2** is then φ_2.

The signal φ_2 can also be generated by using a shift register with feedback similar to those used in the generation of PN sequences for use in spread-spectrum communications. An example of such a shift register is shown in **Figure 11**. The D-latches **D29** through **D32** form a shift register which is clocked by the signal at twice the RF carrier frequency. **MOD1** does a modulo-2 multiplication of the output of **D31** with the output of **D32**, which is then fed into the input of **D32** to produce the required feedback. The signal φ_2 is then produced at the output of **D32**. A similar shift register with similar feedback can be used to produce the signal φ_1. The conditions on the design of these shift registers are that they produce the signals φ_1 and φ_2 that have the properties mentioned above:

- $\varphi_1(t) * \varphi_2(t)$ must have a frequency component at the RF carrier frequency;
- $\varphi_1(t) * \varphi_2(t)$ must not contain a significant amount of power at frequencies other that the RF carrier frequency; and
- $\varphi_1(t)$ and $\varphi_2(t)$ must not contain a significant amount of energy in the RF signal bandwidth.

The signals of the invention may also be generated in many other ways, which would be clear from the teachings herein. For example, φ_1 could be generated using a control signal *S* to selectively divide a 2LO signal by either 2 or by 4. In this case, if the value of *S* is a digital "0" then the 2LO signal could be divided by 2, and if the value of *S* is a digital "1", the 2LO signal could be divided by 4. The function φ_2 can be derived from the control signal *S* in a similar manner, to generate a pair of time-varying signals which meet the criteria of the invention to the extent required by the application.

The invention allows one to fully integrate a RF transmitter on a single chip without using external filters, while furthermore, the RF transmitter can be used as a multi-standard transmitter.

The construction of the necessary logic to generate the mixing signals of the invention would be clear to one skilled in the art from the description herein. Such signals may be generated using basic logic gates, field programmable gate arrays (FPGA), read only memories (ROMs), micro-controllers or other devices known in the art. Though the figures herein imply the use of analogue components, all embodiments can be implemented in digital form.

It would be clear to one skilled in the art that many variations may be made to the designs presented herein, without departing from the spirit of the invention. One such variation to the basic structure in **Figure 3** is to add a filter between the two

mixers **72** and **74** to remove unwanted signals that are transferred to the output port. This filter may be a low pass, high pass, or band pass filter depending on the transmitter requirements, and may be purely passive, or have active components.

In **Figure 3**, two mixer signals are used to perform the down-conversion or up-conversion of *x(t)*. It is also possible to use more than two signals to accomplish the same goal. The block diagram of **Figure 12** presents such a variation, where several functions φ_1, φ_2, φ_3 ... φ_n are used to generate the virtual LO. Here, $\varphi_1 * \varphi_2 * ... * \varphi_n$ has a significant power level at the LO frequency being emulated, but each of the functions $\varphi_1 ... \varphi_n$ contain an insignificant power level at LO. Each of these methods of signal generation can be easily extended to produce more than two signals.

The electrical circuits of the invention may be described by computer software code in a simulation language, or hardware development language used to fabricate integrated circuits. This computer software code may be stored in a variety of formats on various electronic memory media including computer diskettes, CD-ROM, Random Access Memory (RAM) and Read Only Memory (ROM). As well, electronic signals representing such computer software code may also be transmitted via a communication network.

Clearly, such computer software code may also be integrated with the code of other programs, implemented as a core or subroutine by external program calls, or by other techniques known in the art.

The embodiments of the invention may be implemented on various families of integrated circuit technologies using digital signal processors (DSPs), microcontrollers, microprocessors, field programmable gate arrays (FPGAs), or discrete components. Such implementations would be clear to one skilled in the art.

The invention may be applied to various communication protocols and formats including: amplitude modulation (AM), frequency modulation (FM), frequency shift keying (FSK), phase shift keying (PSK), cellular telephone systems including analogue and digital systems such as code division multiple access (CDMA), time division multiple access (TDMA) and frequency division multiple access (FDMA).

The invention may be applied to such applications as wired communication systems include computer communication systems such as local area networks (LANs), point to point signalling, and wide area networks (WANs) such as the Internet, using electrical or optical fibre cable systems. As well, wireless communication systems may include those for public broadcasting such as AM and

FM radio, and UHF and VHF television; or those for private communication such as cellular telephones, personal paging devices, wireless local loops, monitoring of homes by utility companies, cordless telephones including the digital cordless European telecommunication (DECT) standard, mobile radio systems, GSM and AMPS cellular telephones, microwave backbone networks, interconnected appliances under the Bluetooth standard, and satellite communications.

While particular embodiments of the present invention have been shown and described, it is clear that changes and modifications may be made to such embodiments without departing from the true scope and spirit of the invention.

WHAT IS CLAIMED IS:

1. A synthesizer for generating signals to be input to successive mixers for modulating or demodulating an input signal *x(t)*, said synthesizer comprising:

a first signal generator for producing a first time-varying signal φ_1; and

a second signal generator for producing a second time-varying signal φ_2;

where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated.

2. The synthesizer of claim 1, wherein signals used to generate φ_1 and φ_2 do not have a significant amount of power at the output frequency of said output signal $x(t)\ \varphi_1\ \varphi_2$.

3. The synthesizer of claim 2, wherein $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)\ \varphi_1\ \varphi_2$.

4. The synthesizer of claim 3, wherein $\varphi_2 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)\ \varphi_1\ \varphi_2$.

5. The synthesizer of claim 4, wherein said first and second time-varying signals are irregular.

6. The synthesizer of claim 4, wherein said first and second time-varying signals are digital waveforms.

7. The synthesizer of claim 4, wherein said first and second time-varying signals are square waveforms.

8. The synthesizer of claim 4, wherein said first and second time-varying signals are randomly generated.

9. The synthesizer of claim 4, wherein said first and second time-varying signals are pseudo-randomly generated.

10. The synthesizer of claim 4, wherein said first and second time-varying signals are periodic functions of time.

11. The synthesizer of claim 4, wherein said first and second signal generators comprise:

pulse removal means for removing pulses from a local oscillator signal which has a frequency of twice the RF carrier, generating said first time-varying signal φ_1; and

complementary means for generating said second time-varying signal φ_2.

12. The synthesizer of claim 4, wherein said pulse removal means comprises:

a pulse swallower for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and swallowing each pulse with a control signal *S*; and

a divide by two circuit for receiving and dividing said pulse swallowed signal by two, producing said first time-varying signal φ_1.

13. The synthesizer of claim 12, wherein said complementary means comprises:

a delay circuit for receiving and delaying said control signal *S* to be synchronized in time with said first time-varying signal φ_1, outputting said delayed control signal *S* as said second time-varying signal φ_2.

14. The synthesizer of claim 4, wherein said first and second signal generators comprise:

shift register means for generating said first and second time-varying signals φ_1 and φ_2 by shifting out corresponding predetermined sequences.

15. The synthesizer of claim 14, wherein said shift register means comprises:

a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first time-varying signal φ_1, by shifting out a predetermined sequence.

16. The synthesizer of claim 15, wherein said second signal generator comprises:

an exclusive-OR (XOR) circuit for comparing outputs of consecutive latches in said shift register; and

a second shift register being clocked by said XOR output, and generating said second time-varying signal φ_2, by shifting out a second predetermined sequence.

17. The synthesizer of claim 15, wherein said second signal generator comprises:

a third shift register for receiving said oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said second time-varying signal φ_2, by shifting out a predetermined sequence.

18. The synthesizer of claim 4, wherein said first and second signal generators comprise:

means for generating said first time-varying signal φ_1 from an oscillator signal at the frequency of the local oscillator signal being emulated, and a control signal *S* having edges aligned with said oscillator signal; and

means for delaying said control signal *S* to produce said second time-varying signal φ_2.

19. The synthesizer of claim 18, wherein said means for delaying comprises:

a delay latch for sampling said control signal *S* at the frequency of the local oscillator signal being emulated; and

an invertor for receiving and inverting said delay latched control signal *S* to produce said second time-varying signal φ_2.

20. The synthesizer of claim 19, wherein said means for generating said first time-varying signal φ_1 comprises:

a second invertor for receiving the oscillator signal at the frequency of the local oscillator signal being emulated; and

an exclusive-OR (XOR) circuit for comparing said inverted oscillator signal with said latched input signal *x(t)*, producing said first time-varying signal φ_1.

21. The synthesizer of claim 4, wherein said first signal generator comprises:

a shift register with a feedback loop.

22. The synthesizer of claim 21, wherein said first signal generator comprises:

a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first time-varying signal φ_1, by shifting out a predetermined sequence; and

a modulo-2 multiplier for receiving said first time-varying signal φ_1 and the output of an earlier latch in said shift register, feeding an output into a later latch in said shift register.

23. The synthesizer of claim 4 comprising:

one or more additional signal generators for producing one or more additional time-varying signals;

where the product of all of said time-varying signals has significant power at the frequency of a local oscillator signal being emulated, and none of said all of said time-varying signals has significant power at the frequency of said local oscillator signal being emulated.

24. The synthesizer of claim 4, where said first signal generator comprises:

a divide by 2 circuit for receiving an oscillator signal at the frequency of the local oscillator signal being emulated; and

a divide by 4 circuit for receiving said oscillator signal at the frequency of the local oscillator signal being emulated;

selector means for routing either the output of said divide by 2 circuit or said divide by 4 circuit to an output, said output producing said first time-varying signal φ_1.

25. The synthesizer of any one of claims 12, 13, 18, 19 or 24, wherein said control signal S comprises a random signal.

26. The synthesizer of any one of claims 12, 13, 18, 19 or 24, wherein said control signal S comprises a pseudo-random signal.

27. The synthesizer of any one of claims 12, 13, 18, 19 or 24, wherein said control signal S comprises a periodic signal.

28. The synthesizer of any one of claims 12, 13, 18, 19 or 24, comprising:

a delta-sigma (i.e. Δ-S) modulator for generating said control signal *S*.

29. The synthesizer of claim 4 comprising:
first and second latches which are clocked via a common clock, to align said first and second time-varying signals φ_1 and φ_2.

30. An integrated circuit comprising the synthesizer of any one of claims 1 - 29.

31. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the synthesizer of any one of claims 1 - 29.

32. A computer data signal embodied in a output wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio transmitter of any one of claims 1 - 29.

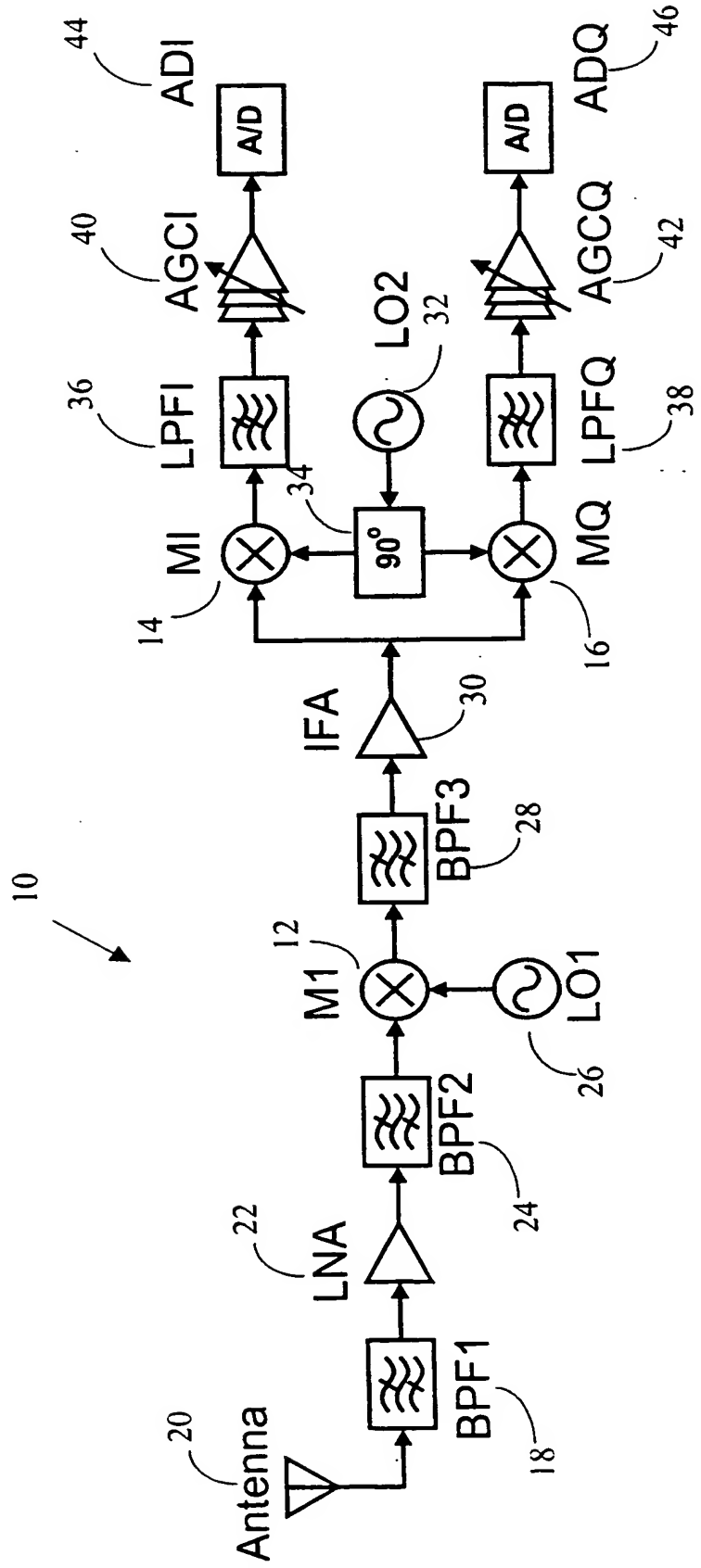


FIGURE 1 - PRIOR ART

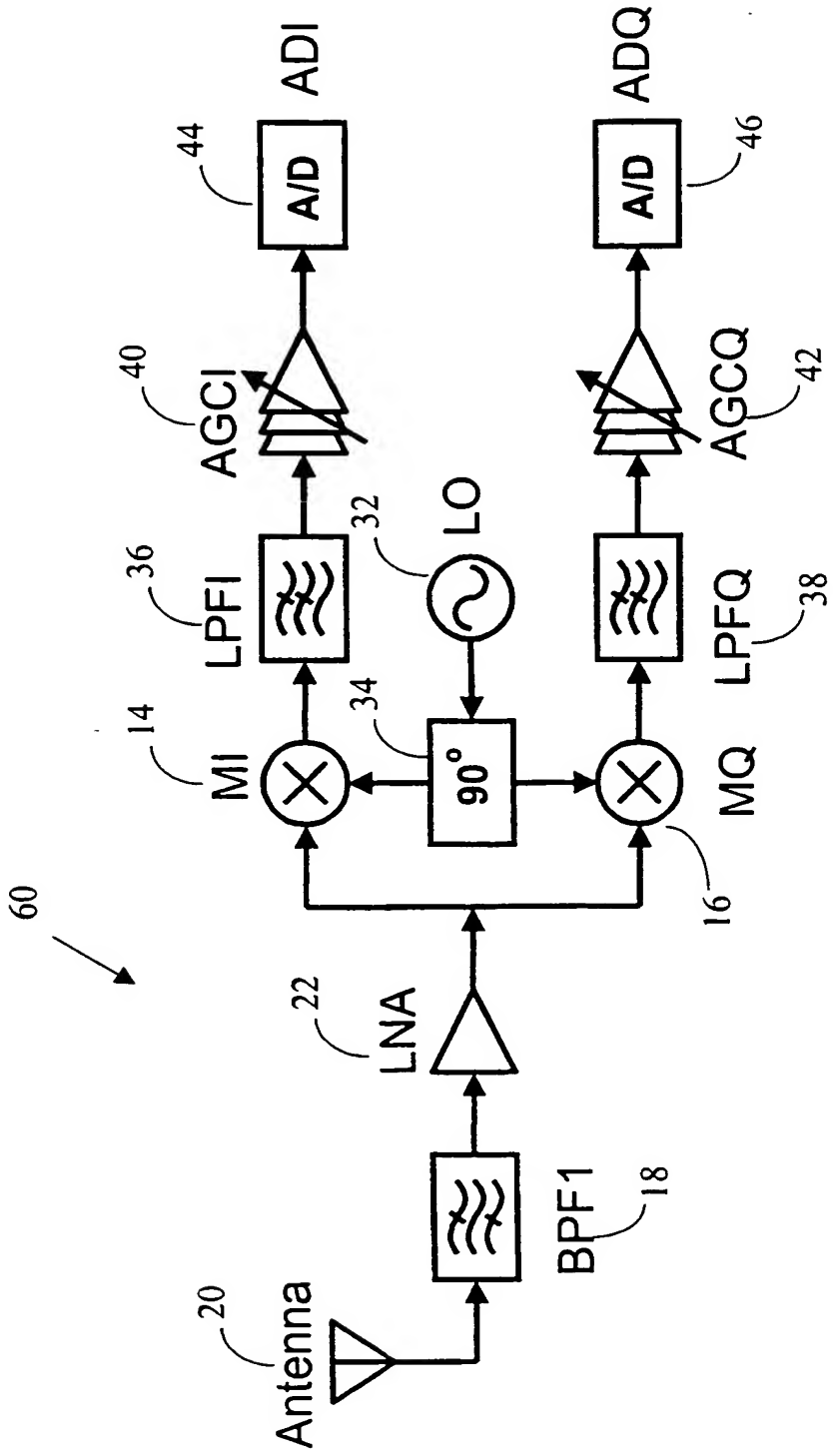


FIGURE 2 - PRIOR ART

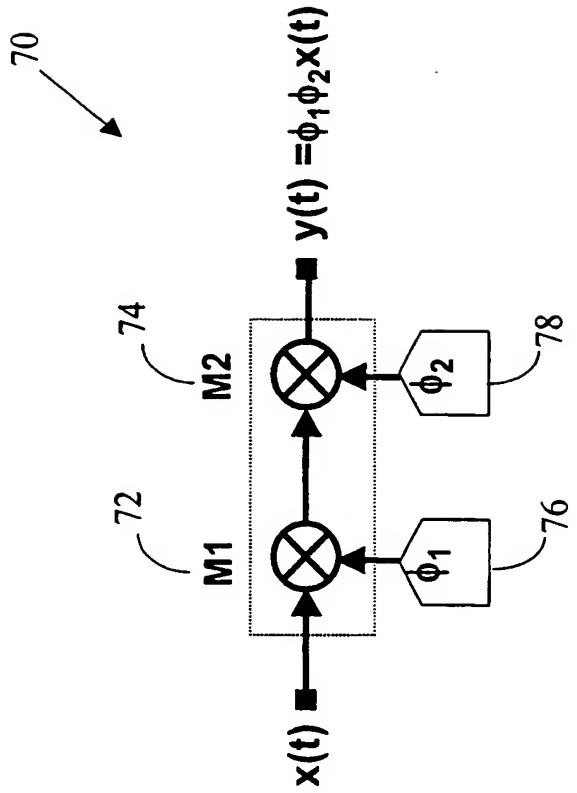


FIGURE 3

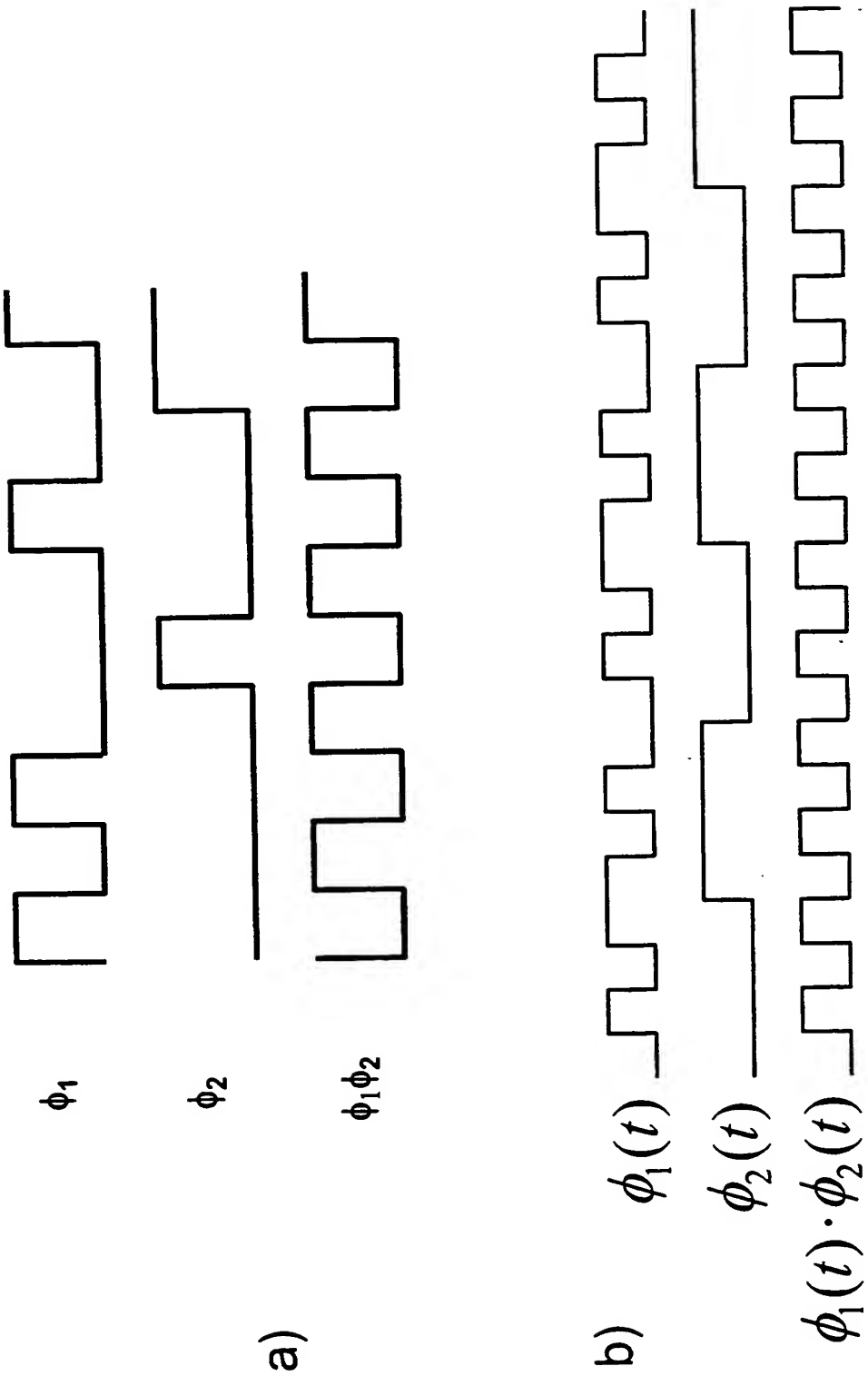


FIGURE 4

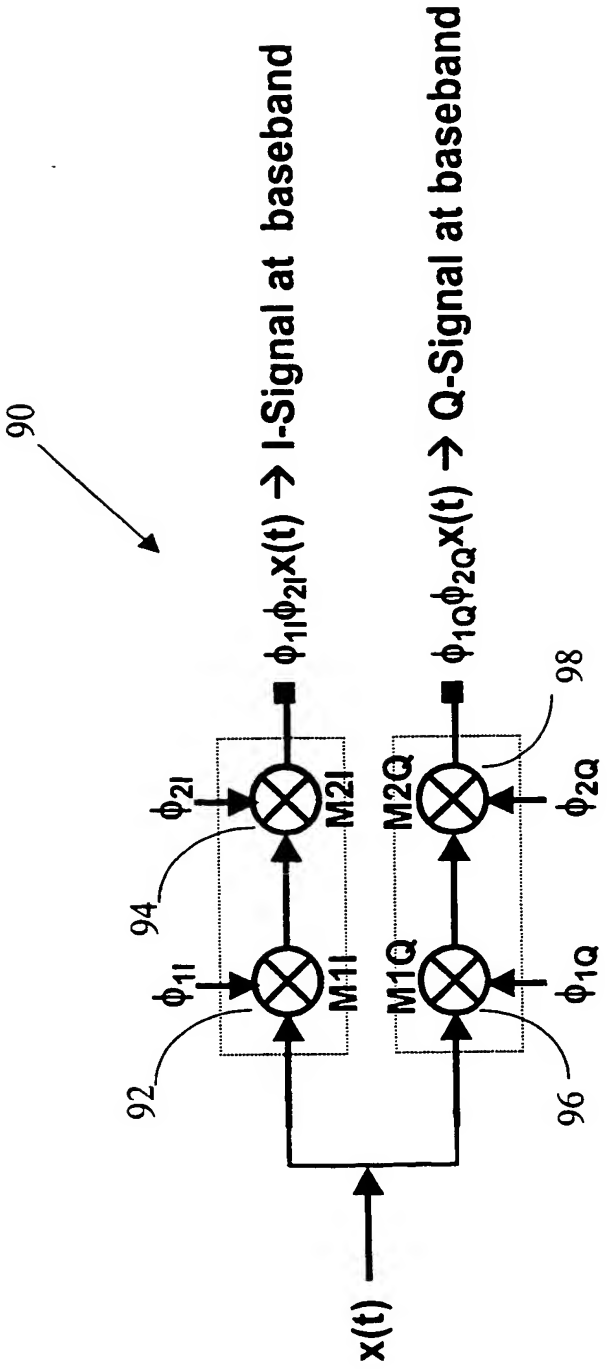

90
$\phi_{1I}\phi_{2I}x(t)$ → I-Signal at baseband
$\phi_{1Q}\phi_{2Q}x(t)$ → Q-Signal at baseband
98
ϕ_{2I}
M2I
M2Q
ϕ_{2Q}
94
ϕ_{1I}
M1I
M1Q
ϕ_{1Q}
92
96
x(t)

FIGURE 5

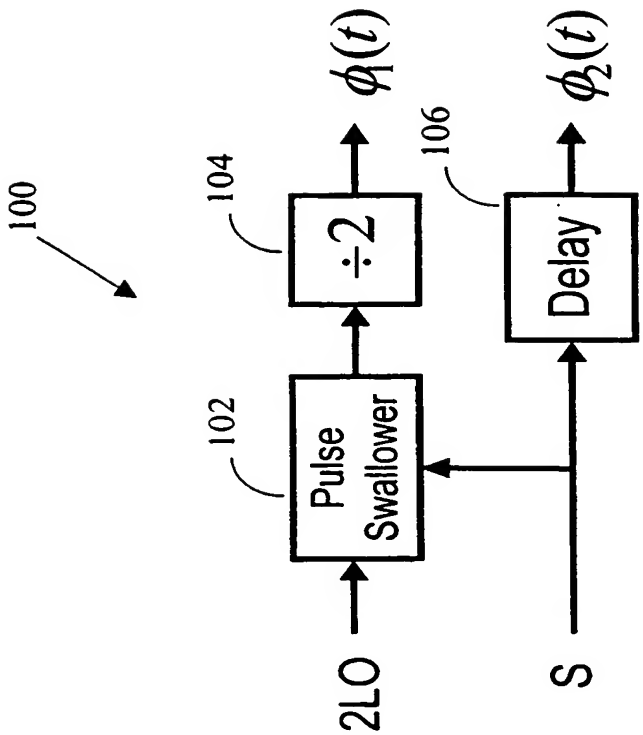


FIGURE 6

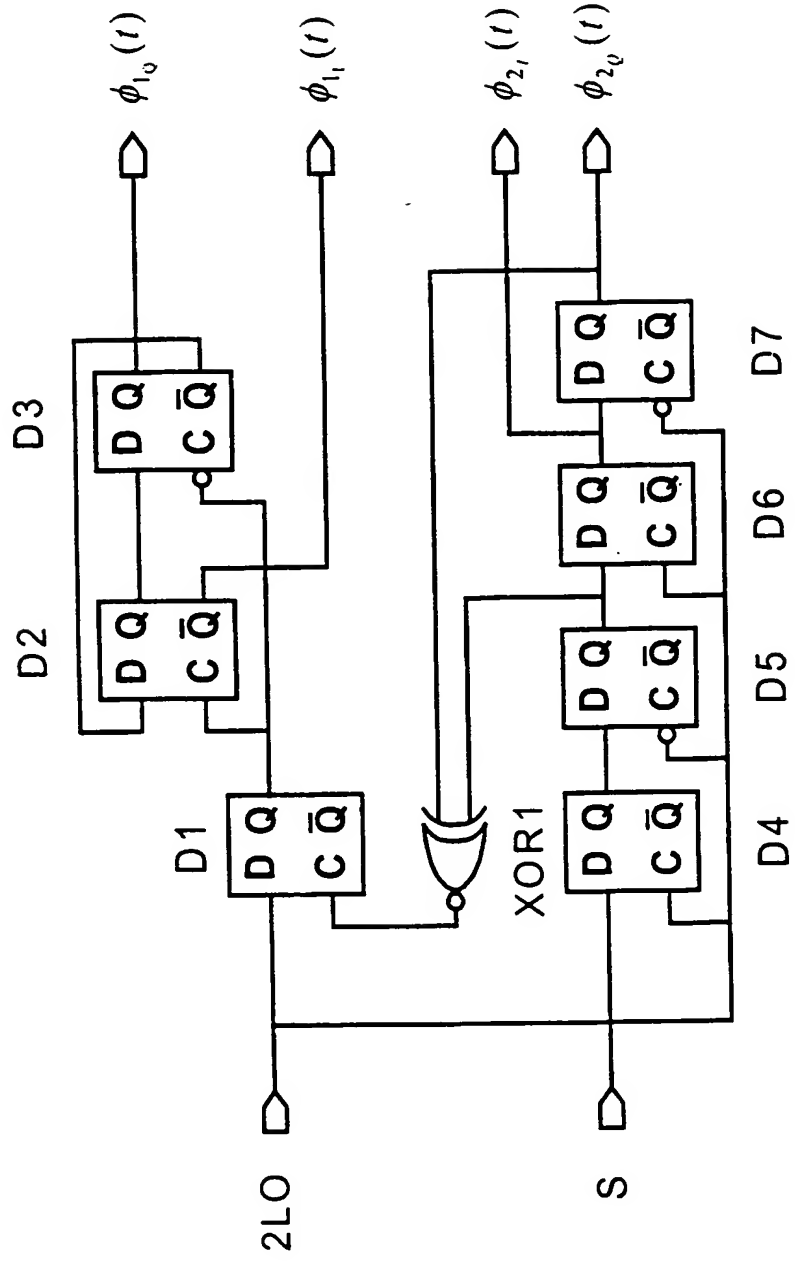


FIGURE 7

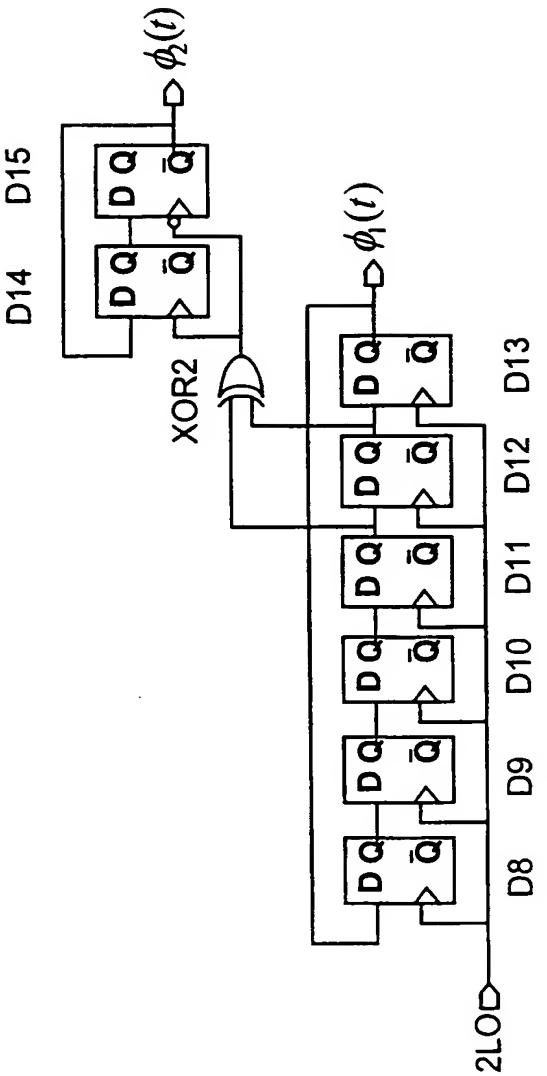


FIGURE 8

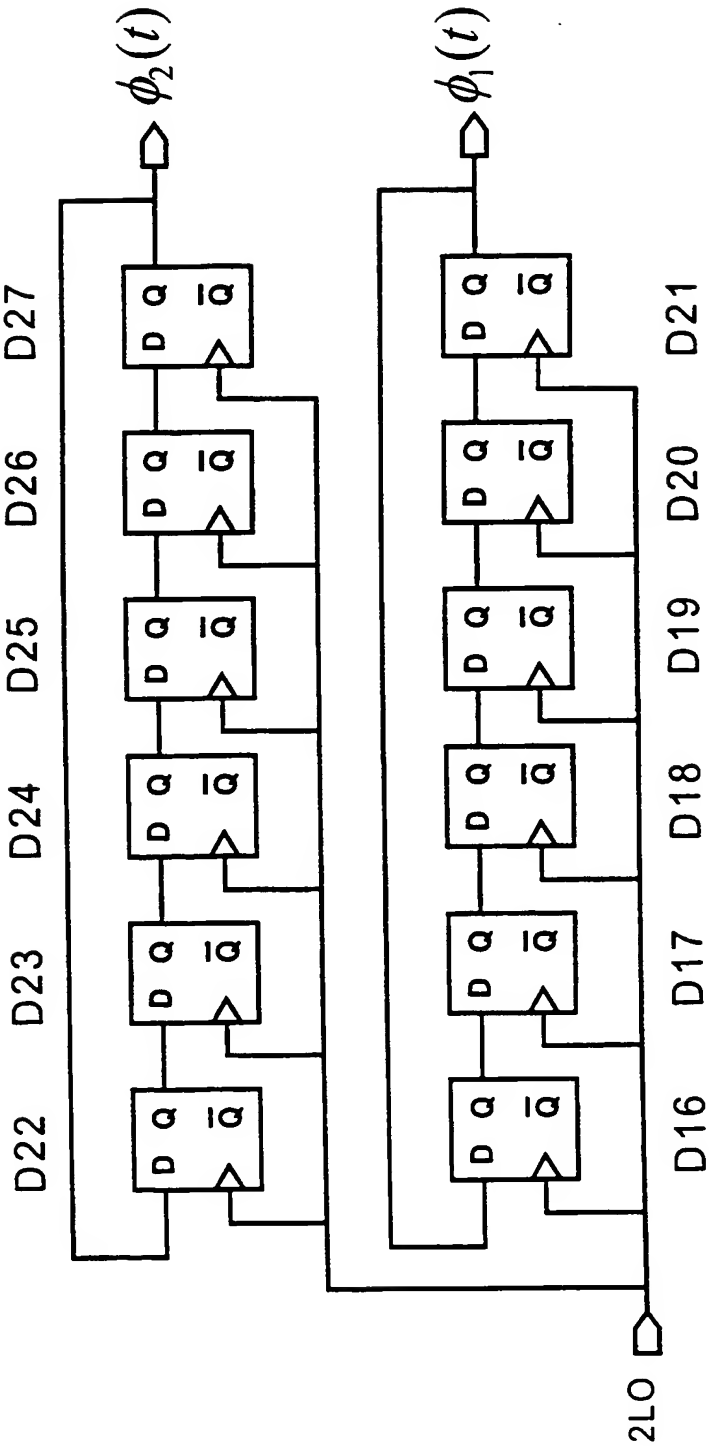

$\phi_2(t)$
$\phi_1(t)$
D27
D26
D25
D24
D23
D22
D21
D20
D19
D18
D17
D16
D
Q
$\overline{Q}$
2LO

FIGURE 9

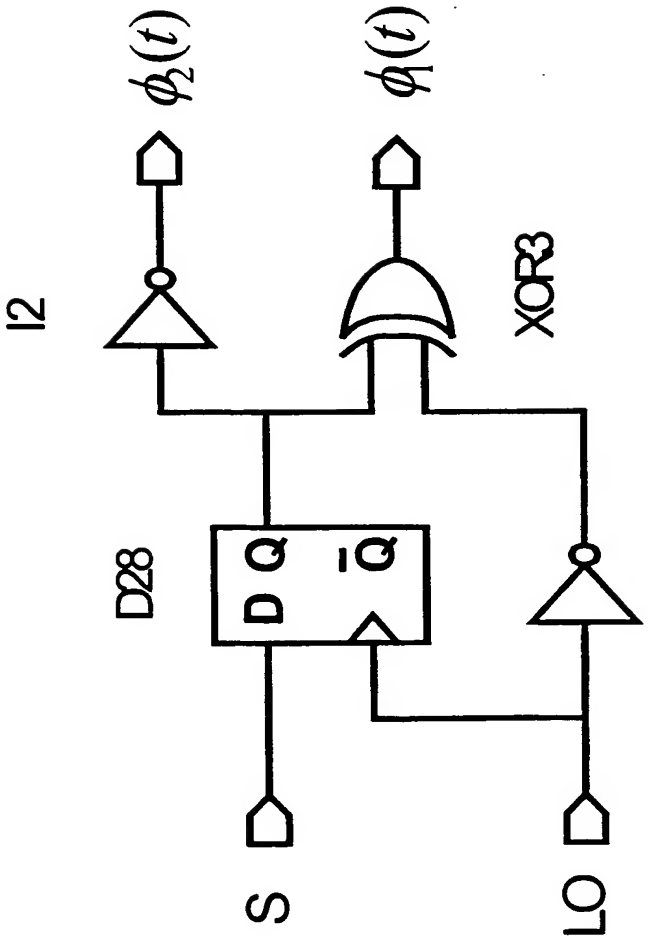


FIGURE 10

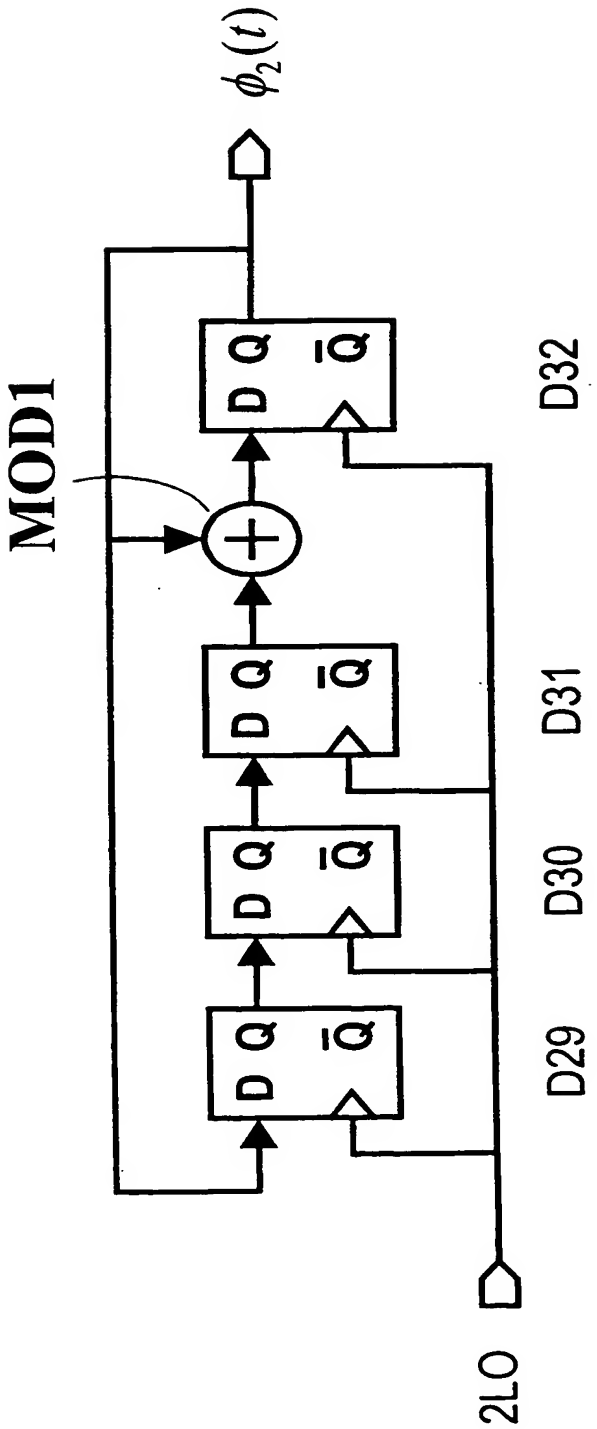


FIGURE 11

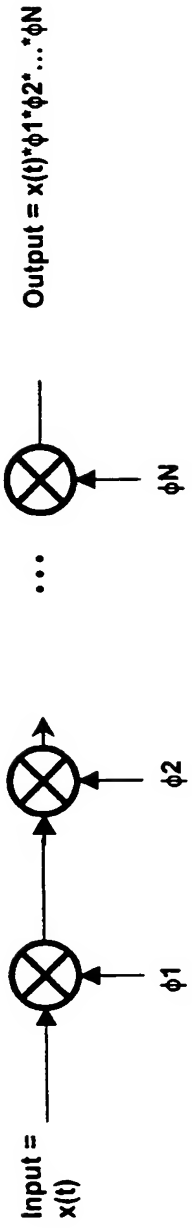


FIGURE 12

INTERNATIONAL SEARCH REPORT

International Application No
PCT/CA 00/00996

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04B1/26 H04B1/28 H03D7/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04B H03D

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 96 01006 A (HONEYWELL INC) 11 January 1996 (1996-01-11) abstract page 2, line 1 - line 16 page 4, line 5 - line 22 claims 1-7; figure 2	1-10
X	EP 0 899 868 A (MITEL CORP) 3 March 1999 (1999-03-03) abstract column 1, line 22 - line 42 claims 1-6	1-10

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 January 2001	24/01/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Lazaridis, P

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/CA 00/00996

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9601006 A	11-01-1996	AU 2909795 A	25-01-1996
EP 0899868 A	03-03-1999	CA 2245958 A	28-02-1999

WHAT IS CLAIMED IS:

1. A synthesizer for generating signals to be input to successive mixers for modulating or demodulating an input signal *x(t)*, said synthesizer comprising:

a first signal generator for producing a first time-varying signal φ_1; and

a second signal generator for producing a second time-varying signal φ_2;

where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated.

2. The synthesizer of claim 1, wherein signals used to generate φ_1 and φ_2 do not have a significant amount of power at the output frequency of said output signal $x(t)$ φ_1 φ_2.

3. The synthesizer of claim 2, wherein $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)$ φ_1 φ_2.

4. The synthesizer of claim 3, wherein $\varphi_2 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)$ φ_1 φ_2.

5. The synthesizer of claim 4, wherein said first and second time-varying signals are irregular.

6. The synthesizer of claim 4, wherein said first and second time-varying signals are digital waveforms.

7. The synthesizer of claim 4, wherein said first and second time-varying signals are square waveforms.

8. The synthesizer of claim 4, wherein said first and second time-varying signals are randomly generated.

9. The synthesizer of claim 4, wherein said first and second time-varying signals are pseudo-randomly generated.

10. The synthesizer of claim 4, wherein said first and second time-varying signals are periodic functions of time.

11. The synthesizer of claim 4, wherein said first and second signal generators comprise:

pulse removal means for removing pulses from a local oscillator signal which has a frequency of twice the RF carrier, generating said first time-varying signal φ_1; and

complementary means for generating said second time-varying signal φ_2.

12. The synthesizer of claim 4, wherein said pulse removal means comprises:

a pulse swallower for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and swallowing each pulse with a control signal *S*; and

a divide by two circuit for receiving and dividing said pulse swallowed signal by two, producing said first time-varying signal φ_1.

13. The synthesizer of claim 12, wherein said complementary means comprises:

a delay circuit for receiving and delaying said control signal *S* to be synchronized in time with said first time-varying signal φ_1, outputting said delayed control signal *S* as said second time-varying signal φ_2.

14. The synthesizer of claim 4, wherein said first and second signal generators comprise:

shift register means for generating said first and second time-varying signals φ_1 and φ_2 by shifting out corresponding predetermined sequences.

15. The synthesizer of claim 14, wherein said shift register means comprises:

a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first time-varying signal φ_1, by shifting out a predetermined sequence.

16. The synthesizer of claim 15, wherein said second signal generator comprises:

an exclusive-OR (XOR) circuit for comparing outputs of consecutive latches in said shift register; and

a second shift register being clocked by said XOR output, and generating said second time-varying signal φ_2, by shifting out a second predetermined sequence.

17. The synthesizer of claim 15, wherein said second signal generator comprises:

a third shift register for receiving said oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said second time-varying signal φ_2, by shifting out a predetermined sequence.

18. The synthesizer of claim 4, wherein said first and second signal generators comprise:

means for generating said first time-varying signal φ_1 from an oscillator signal at the frequency of the local oscillator signal being emulated, and a control signal *S* having edges aligned with said oscillator signal; and

means for delaying said control signal *S* to produce said second time-varying signal φ_2.

19. The synthesizer of claim 18, wherein said means for delaying comprises:

a delay latch for sampling said control signal *S* at the frequency of the local oscillator signal being emulated; and

an invertor for receiving and inverting said delay latched control signal *S* to produce said second time-varying signal φ_2.

20. The synthesizer of claim 19, wherein said means for generating said first time-varying signal φ_1 comprises:

a second invertor for receiving the oscillator signal at the frequency of the local oscillator signal being emulated; and

an exclusive-OR (XOR) circuit for comparing said inverted oscillator signal with said latched input signal *x(t)*, producing said first time-varying signal φ_1.

21. The synthesizer of claim 4, wherein said first signal generator comprises:

a shift register with a feedback loop.

22. The synthesizer of claim 21, wherein said first signal generator comprises:

a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first time-varying signal φ_1, by shifting out a predetermined sequence; and

a modulo-2 multiplier for receiving said first time-varying signal φ_1 and the output of an earlier latch in said shift register, feeding an output into a later latch in said shift register.

23. The synthesizer of claim 4 comprising:

one or more additional signal generators for producing one or more additional time-varying signals;

where the product of all of said time-varying signals has significant power at the frequency of a local oscillator signal being emulated, and none of said all of said time-varying signals has significant power at the frequency of said local oscillator signal being emulated.

24. The synthesizer of claim 4, where said first signal generator comprises:

a divide by 2 circuit for receiving an oscillator signal at the frequency of the local oscillator signal being emulated; and

a divide by 4 circuit for receiving said oscillator signal at the frequency of the local oscillator signal being emulated;

selector means for routing either the output of said divide by 2 circuit or said divide by 4 circuit to an output, said output producing said first time-varying signal φ_1.

25. The synthesizer of any one of claims 12, 13, 18, 19 or 24, wherein said control signal S comprises a random signal.

26. The synthesizer of any one of claims 12, 13, 18, 19 or 24, wherein said control signal S comprises a pseudo-random signal.

27. The synthesizer of any one of claims 12, 13, 18, 19 or 24, wherein said control signal S comprises a periodic signal.

28. The synthesizer of any one of claims 12, 13, 18, 19 or 24, comprising:

a delta-sigma (i.e. Δ-S) modulator for generating said control signal *S*.

29. The synthesizer of claim 4 comprising:
first and second latches which are clocked via a common clock, to align said first and second time-varying signals φ_1 and φ_2.

30. An integrated circuit comprising the synthesizer of any one of claims 1 - 29.

31. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the synthesizer of any one of claims 1 - 29.

32. A computer data signal embodied in a output wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio transmitter of any one of claims 1 - 29.

PATENT COOPERATION TREATY

From the:
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:
HARRIS, J.D.
Gowling Lafleur Henderson LLP
Suite 2600
160 Elgin Street
Ottawa, Ontario K1P 1C3
CANADA

PCT

WRITTEN OPINION

(PCT Rule 66)

Date of mailing *(day/month/year)*	17.07.2001
Applicant's or agent's file reference: 08-887955WO	**REPLY DUE** **within 3 month(s)** from the above date of mailing

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/CA00/00996	01/09/2000	01/09/1999

International Patent Classification (IPC) or both national classification and IPC
H04B1/26

Applicant
SIRIFIC WIRELESS CORPORATION et al.

1. This written opinion is the **first** drawn up by this International Preliminary Examining Authority.

2. This opinion contains indications relating to the following items:

I	☒	Basis of the opinion
II	☐	Priority
III	☐	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
IV	☐	Lack of unity of invention
V	☒	Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
VI	☐	Certain document cited
VII	☒	Certain defects in the international application
VIII	☒	Certain observations on the international application

3. The applicant is hereby **invited to reply** to this opinion.

When? See the time limit indicated above. The applicant may, before the expiration of that time limit, request this Authority to grant an extension, see Rule 66.2(d).

How? By submitting a written reply, accompanied, where appropriate, by amendments, according to Rule 66.3. For the form and the language of the amendments, see Rules 66.8 and 66.9.

Also: For an additional opportunity to submit amendments, see Rule 66.4.
For the examiner's obligation to consider amendments and/or arguments, see Rule 66.4 bis.
For an informal communication with the examiner, see Rule 66.6.

If no reply is filed, the international preliminary examination report will be established on the basis of this opinion.

4. The final date by which the international preliminary examination report must be established according to Rule 69.2 is: 01/01/2002.

Name and mailing address of the international preliminary examining authority:
European Patent Office
D-80298 Munich
Tel. +49 89 2399 - 0 Tx: 523656 epmu d
Fax: +49 89 2399 - 4465

Authorized officer / Examiner
Kolbe, W

Formalities officer (incl. extension of time limits)
Kiepe, C
Telephone No. +49 89 2399 2423

I. Basis of the opinion

1. With regard to the **elements** of the international application (Replacement *sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this opinion as "originally filed"*):

Description, pages:

1-18 as originally filed

Claims, No.:

1-32 as originally filed

Drawings, sheets:

1/12-12/12 as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language: , which is:

- ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
- ☐ the language of publication of the international application (under Rule 48.3(b)).
- ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- ☐ contained in the international application in written form.
- ☐ filed together with the international application in computer readable form.
- ☐ furnished subsequently to this Authority in written form.
- ☐ furnished subsequently to this Authority in computer readable form.
- ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
- ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:

☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

(Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1
Inventive step (IS)	Claims	2-32
Industrial applicability (IA)	Claims	

2. Citations and explanations
see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:
see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:
see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Reference is made to the following documents:
   D1: WO 96 01006 A (HONEYWELL INC) 11 January 1996 (1996-01-11)
   D2: EP-A-0 899 868 (MITEL CORP) 3 March 1999 (1999-03-03)

2. Document D1, see in particular the passages cited in the search report, discloses as in claim 1:
   A synthesizer for generating signals to be input to successive mixers (21,26) for modulating or demodulating an input signal (80 MHz R.F.), said synthesizer 22,24,27,28) comprising a first signal generator (22) for producing a first time-varying signal φ1 and a second signal generator (27) for producing a second time-varying signal φ2; where φ1*φ2 has significant power at the frequency (i.e. 81 MHz) of the local oscillator being emulated, and neither φ1 nor φ2 has significant power at the frequency of said local oscillator being emulated.

   The references in parentheses apply to the figures of D1.

   Since all the features of claim 1 are known from D1, the claim lacks novelty in the sense of Article 33(1),(2) PCT.

   It should be noted that any two stage mixer falls into the scope of claim 1, since every local oscillator produces a "time-varying signal" because the voltage of such a signal varies in time (periodically, see page 10, line 1) with the frequency of the oscillator.

3. Dependent claims 2 to 32 do not appear to contain any additional features which, in combination with the features of any claim to which they refer, involve an inventive step (Article 56 EPC) since these claims merely define an association of known features functioning in their normal way and, in combination, not producing any non-obvious working interrelationship, cf. Guidelines C-IV,8.8 (B1).

Re Item VII

Certain defects in the international application

1. The features of the claims are not provided with reference signs placed in parentheses (Rule 6.2(b) PCT).

2. Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the documents D1 to D2 is not mentioned in the description, nor are these documents identified therein.

3. If an amended set of claims is filed, then the description has to be adapted accordingly. The applicant is further requested to provide clear indication from where in the original application the amendments were derived, cf. Article 19(2) PCT.

Re Item VIII

Certain observations on the international application

1. Claim 1 tries to define the synthesizer using parameters (the power at the frequency of a local oscillator being emulated) which are unsuitable to clearly define the structure of the synthesizer to be protected. Claim 1 is thus unclear in the sense of Article 6 PCT. To address @ National Entry.

2. Claims 2 to 4 try to define the synthesizer by reference to the input signal x(t) which may be applied to the mixers for which the signals of the synthesizer are intended. Such a definition is unsuitable to define the structure of the synthesizer. These claims are thus unclear, Article 6 PCT.

desired input signal
input signal to be demodulated
simply "input"?

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70) 12

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
08-887955WO		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/CA00/00996	01/09/2000	01/09/1999
International Patent Classification (IPC) or national classification and IPC H04B1/26		
Applicant SIRIFIC WIRELESS CORPORATION et al.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 5 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☒ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
29/03/2001	17.01.2002
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Kolbe, W Telephone No. +49 89 2399 8479

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/CA00/00996

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:
Description, pages:

1-18	as originally filed

Claims, No.:

1-33	as received on	17/12/2001	with letter of	17/12/2001

Drawings, sheets:

1/12-12/12	as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

   These elements were available or furnished to this Authority in the following language: , which is:

   - ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
   - ☐ the language of publication of the international application (under Rule 48.3(b)).
   - ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

   - ☐ contained in the international application in written form.
   - ☐ filed together with the international application in computer readable form.
   - ☐ furnished subsequently to this Authority in written form.
   - ☐ furnished subsequently to this Authority in computer readable form.
   - ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
   - ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

   - ☐ the description, pages:
   - ☐ the claims, Nos.:

☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	2-33
	No:	Claims	1
Inventive step (IS)	Yes:	Claims	
	No:	Claims	2-33
Industrial applicability (IA)	Yes:	Claims	1-33
	No:	Claims	

2. Citations and explanations
   see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:
see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:
see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Reference is made to the following documents:
   D1: WO 96 01006 A (HONEYWELL INC) 11 January 1996 (1996-01-11)
   D2: EP-A-0 899 868 (MITEL CORP) 3 March 1999 (1999-03-03)

2. Document D1, see in particular the passages cited in the search report, discloses as in claim 1:

   A synthesizer for generating signals to be input to successive mixers (21,26) for modulating or demodulating an input signal (80 MHz R.F.), said synthesizer 22,24,27,28) comprising a first signal generator (22) for producing a first mixing signal φ1 which varies irregularly over time and a second signal generator (27) for producing a second mixing signal φ2 which varies irregularly over time; where φ1*φ2 has significant power at the frequency (i.e. 81 MHz) of the local oscillator being emulated, and neither φ1 nor φ2 has significant power at the frequency of said local oscillator being emulated (the spreading will not produce significant energy at 81 MHz).

   The references in parentheses apply to the figures of D1.

   It should be noted that the structure claimed by claim 1 is identical to the structure disclosed by D1 in its claim 1 which does not provide any additional filters.

   Since all the features of claim 1 are known from D1, the claim lacks novelty in the sense of Article 33(1),(2) PCT.

3. Dependent claims 2 to 33 do not appear to contain any additional features which, in combination with the features of any claim to which they refer, involve an inventive step (Article 56 EPC) since these claims merely define an association of known features functioning in their normal way and, in combination, not producing any non-obvious working interrelationship, cf. Guidelines C-IV,8.8 (B1).

Re Item VII

Certain defects in the international application

Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the documents D1 to D2 is not mentioned in the description, nor are these documents identified therein.

Re Item VIII

Certain observations on the international application

1. Claim 1 tries to define the synthesizer using parameters (the power at the frequency of a local oscillator being emulated) which are unsuitable to clearly define the structure of the synthesizer to be protected. Claim 1 is thus unclear in the sense of Article 6 PCT.

2. Claims 2 to 4 try to define the synthesizer by reference to the input signal x(t) which may be applied to the mixers for which the signals of the synthesizer are intended. Such a definition is unsuitable to define the structure of the synthesizer. These claims are thus unclear, Article 6 PCT.

PATENT COOPERATION TREATY

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:

HARRIS, J.D.
Gowling Lafleur Henderson LLP
Suite 2600
160 Elgin Street
Ottawa, Ontario K1P 1C3
CANADA

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL PRELIMINARY EXAMINATION REPORT
(PCT Rule 71.1)

Date of mailing *(day/month/year)*	17.01.2002
Applicant's or agent's file reference: 08-887955WO	**IMPORTANT NOTIFICATION**

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/CA00/00996	01/09/2000	01/09/1999

Applicant
SIRIFIC WIRELESS CORPORATION et al.

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices) (Article 39(1)) (see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

Name and mailing address of the IPEA/	Authorized officer
European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Teschauer, B Tel.+49 89 2399-8231

Form PCT/IPEA/416 (July 1992)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant's or agent's file reference	FOR FURTHER ACTION	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
08-887955WO		
International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/CA00/00996	01/09/2000	01/09/1999

International Patent Classification (IPC) or national classification and IPC
H04B1/26

Applicant
SIRIFIC WIRELESS CORPORATION et al.

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

   ☒ This report is also accompanied by ANNEXES, i.e. sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

   These annexes consist of a total of 5 sheets.

3. This report contains indications relating to the following items:

   - I ☒ Basis of the report
   - II ☐ Priority
   - III ☐ Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
   - IV ☐ Lack of unity of invention
   - V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations suporting such statement
   - VI ☐ Certain documents cited
   - VII ☒ Certain defects in the international application
   - VIII ☒ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
29/03/2001	17.01.2002
Name and mailing address of the international preliminary examining authority: European Patent Office D-80298 Munich Tel. +49 89 2399 - 0 Tx: 523656 epmu d Fax: +49 89 2399 - 4465	Authorized officer Kolbe, W Telephone No. +49 89 2399 8479

Form PCT/IPEA/409 (cover sheet) (January 1994)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No. PCT/CA00/00996

I. Basis of the report

1. With regard to the **elements** of the international application *(Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17))*:
Description, pages:

1-18 as originally filed

Claims, No.:

1-33 as received on 17/12/2001 with letter of 17/12/2001

Drawings, sheets:

1/12-12/12 as originally filed

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.

These elements were available or furnished to this Authority in the following language: , which is:

- ☐ the language of a translation furnished for the purposes of the international search (under Rule 23.1(b)).
- ☐ the language of publication of the international application (under Rule 48.3(b)).
- ☐ the language of a translation furnished for the purposes of international preliminary examination (under Rule 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

- ☐ contained in the international application in written form.
- ☐ filed together with the international application in computer readable form.
- ☐ furnished subsequently to this Authority in written form.
- ☐ furnished subsequently to this Authority in computer readable form.
- ☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.
- ☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. The amendments have resulted in the cancellation of:

- ☐ the description, pages:
- ☐ the claims, Nos.:

☐ the drawings, sheets:

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed (Rule 70.2(c)):

   (Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.)

6. Additional observations, if necessary:

V. Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Yes:	Claims	2-33
	No:	Claims	1
Inventive step (IS)	Yes:	Claims	
	No:	Claims	2-33
Industrial applicability (IA)	Yes:	Claims	1-33
	No:	Claims	

2. Citations and explanations
   see separate sheet

VII. Certain defects in the international application

The following defects in the form or contents of the international application have been noted:
see separate sheet

VIII. Certain observations on the international application

The following observations on the clarity of the claims, description, and drawings or on the question whether the claims are fully supported by the description, are made:
see separate sheet

Re Item V

Reasoned statement with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Reference is made to the following documents:
   D1: WO 96 01006 A (HONEYWELL INC) 11 January 1996 (1996-01-11)
   D2: EP-A-0 899 868 (MITEL CORP) 3 March 1999 (1999-03-03)

2. Document D1, see in particular the passages cited in the search report, discloses as in claim 1:

   A synthesizer for generating signals to be input to successive mixers (21,26) for modulating or demodulating an input signal (80 MHz R.F.), said synthesizer 22,24,27,28) comprising a first signal generator (22) for producing a first mixing signal φ1 which varies irregularly over time and a second signal generator (27) for producing a second mixing signal φ2 which varies irregularly over time; where φ1*φ2 has significant power at the frequency (i.e. 81 MHz) of the local oscillator being emulated, and neither φ1 nor φ2 has significant power at the frequency of said local oscillator being emulated (the spreading will not produce significant energy at 81 MHz).

   The references in parentheses apply to the figures of D1.

   It should be noted that the structure claimed by claim 1 is identical to the structure disclosed by D1 in its claim 1 which does not provide any additional filters.

   Since all the features of claim 1 are known from D1, the claim lacks novelty in the sense of Article 33(1),(2) PCT.

3. Dependent claims 2 to 33 do not appear to contain any additional features which, in combination with the features of any claim to which they refer, involve an inventive step (Article 56 EPC) since these claims merely define an association of known features functioning in their normal way and, in combination, not producing any non-obvious working interrelationship, cf. Guidelines C-IV,8.8 (B1).

Re Item VII

Certain defects in the international application

Contrary to the requirements of Rule 5.1(a)(ii) PCT, the relevant background art disclosed in the documents D1 to D2 is not mentioned in the description, nor are these documents identified therein.

Re Item VIII

Certain observations on the international application

1. Claim 1 tries to define the synthesizer using parameters (the power at the frequency of a local oscillator being emulated) which are unsuitable to clearly define the structure of the synthesizer to be protected. Claim 1 is thus unclear in the sense of Article 6 PCT.

2. Claims 2 to 4 try to define the synthesizer by reference to the input signal x(t) which may be applied to the mixers for which the signals of the synthesizer are intended. Such a definition is unsuitable to define the structure of the synthesizer. These claims are thus unclear, Article 6 PCT.

WHAT IS CLAIMED IS:

1. A synthesizer for generating signals to be input to successive mixers for modulating or demodulating an input signal $x(t)$, said synthesizer comprising:

a first signal generator for producing a first mixing signal φ_1 which varies irregularly over time; and

a second signal generator for producing a second mixing signal φ_2 which varies irregularly over time;

where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated.

2. The synthesizer of claim 1, wherein signals used to generate φ_1 and φ_2 do not have a significant amount of power at the output frequency of said output signal $x(t)$ φ_1, φ_2.

3. The synthesizer of claim 2, wherein $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)$ φ_1, φ_2.

4. The synthesizer of claim 3, wherein $\varphi_2 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)$ φ_1, φ_2.

5. The synthesizer of claim 4, wherein said first and second mixing signals φ_1 and φ_2 are generating using a single time base.

6. The synthesizer of claim 4, wherein said first and second mixing signals φ_1 and φ_2 are digital waveforms.

7. The synthesizer of claim 4, wherein said first and second mixing signals φ_1 and φ_2 are square waveforms.

8. The synthesizer of claim 4, wherein said first and second mixing signals φ_1 and φ_2 are randomly generated.

9. The synthesizer of claim 4, wherein said first and second mixing signals φ_1 and φ_2 are pseudo-randomly generated.

10. The synthesizer of claim 4, wherein said first and second mixing signals φ_1 and φ_2 are periodic functions of time.

11. The synthesizer of claim 4, wherein said first and second signal generators comprise:

pulse removal means for removing pulses from a local oscillator signal which has a frequency of twice the RF carrier, generating said first mixing signal φ_1; and

complementary means for generating said second mixing signal φ_2.

12. The synthesizer of claim 4, wherein said pulse removal means comprises:

a pulse swallower for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and swallowing each pulse with a control signal *S*; and

a divide by two circuit for receiving and dividing said pulse swallowed signal by two, producing said first mixing signal φ_1.

13. The synthesizer of claim 12, wherein said complementary means comprises:

a delay circuit for receiving and delaying said control signal *S* to be synchronized in time with said first mixing signal φ_1, outputting said delayed control signal *S* as said second mixing signal φ_2.

14. The synthesizer of claim 4, wherein said first and second signal generators comprise:

shift register means for generating said first and second mixing signals φ_1 and φ_2 by shifting out corresponding predetermined sequences.

15. The synthesizer of claim 14, wherein said shift register means comprises:

a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first mixing signal φ_1, by shifting out a predetermined sequence.

16. The synthesizer of claim 15, wherein said second signal generator comprises:

an exclusive-OR (XOR) circuit for comparing outputs of consecutive latches in said shift register; and

a second shift register being clocked by said XOR output, and generating said second mixing signal φ_2, by shifting out a second predetermined sequence.

17. The synthesizer of claim 15, wherein said second signal generator comprises:

a third shift register for receiving said oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said second mixing signal φ_2, by shifting out a predetermined sequence.

18. The synthesizer of claim 4, wherein said first and second signal generators comprise:

means for generating said first mixing signal φ_1 from an oscillator signal at the frequency of the local oscillator signal being emulated, and a control signal *S* having edges aligned with said oscillator signal; and

means for delaying said control signal *S* to produce said second mixing signal φ_2.

19. The synthesizer of claim 18, wherein said means for delaying comprises:

a delay latch for sampling said control signal *S* at the frequency of the local oscillator signal being emulated; and

an invertor for receiving and inverting said delay latched control signal *S* to produce said second mixing signal φ_2.

20. The synthesizer of claim 19, wherein said means for generating said first mixing signal φ_1 comprises:

a second invertor for receiving the oscillator signal at the frequency of the local oscillator signal being emulated; and

an exclusive-OR (XOR) circuit for comparing said inverted oscillator signal with said latched input signal *x(t)*, producing said first mixing signal φ_1.

21. The synthesizer of claim 4, wherein said first signal generator comprises:

a shift register with a feedback loop.

22. The synthesizer of claim 21, wherein said first signal generator comprises:

a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first mixing signal φ_1, by shifting out a predetermined sequence; and

a modulo-2 multiplier for receiving said first mixing signal φ_1 and the output of an earlier latch in said shift register, feeding an output into a later latch in said shift register.

23. The synthesizer of claim 4 comprising:

one or more additional signal generators for producing one or more additional mixing signals, varying irregularly over time;

where the product of all of said mixing signals has significant power at the frequency of a local oscillator signal being emulated, and none of said all of said mixing signals has significant power at the frequency of said local oscillator signal being emulated.

24. The synthesizer of claim 4, where said first signal generator comprises:

a divide by 2 circuit for receiving an oscillator signal at the frequency of the local oscillator signal being emulated; and

a divide by 4 circuit for receiving said oscillator signal at the frequency of the local oscillator signal being emulated;

selector means for routing either the output of said divide by 2 circuit or said divide by 4 circuit to an output, said output producing said first mixing signal φ_1

25. The synthesizer of any one of claims 12, 13, 18, 19 or 20, wherein said control signal S comprises a random signal.

26. The synthesizer of any one of claims 12, 13, 18, 19 or 20, wherein said control signal S comprises a pseudo-random signal.

27. The synthesizer of any one of claims 12, 13, 18, 19 or 20, wherein said control signal S comprises a periodic signal.

28. The synthesizer of any one of claims 12, 13, 18, 19 or 20, comprising:

a delta-sigma (Δ-S) modulator for generating said control signal *S*.

29. The synthesizer of claim 4 comprising:

first and second latches which are clocked via a common clock, to align said first and second mixing signals φ_1 and φ_2.

30. The synthesizer of claim 4, wherein the patterns of said first and second mixing signals φ_1 and φ_2 are different from one another.

31. An integrated circuit comprising the synthesizer of any one of claims 1 - 30.

32. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the synthesizer of any one of claims 1 - 30.

33. A computer data signal embodied in a output wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio transmitter of any one of claims 1 - 30.

IN THE EUROPEAN PATENT OFFICE

The International Preliminary Examining Authority

In The Matter of International (PCT) Patent Application:

Applicant	: **SiRiFIC Wireless Corporation; et al.**
Serial No.	: **PCT/CA00/00996**
Filing Date	: **September 1, 2000**
Title	: **Improved Method And Apparatus For Up- and Down-Conversion Of Radio Frequency (RF) Signals**
Our File	: **08887955WO**
Date	: **December 17, 2001**

European Patent Office
Erhardstrasse 27
D-80298 Munich
FEDERAL REPUBLIC OF GERMANY

Response to Written Opinion

Dear Sir:

In response to the Written Opinion dated July 17, 2001, kindly amend this application as follows:

In the Claims:

Substitute the attached claims pages 35 - 36, containing amended claims 12 - 21 for the corresponding pages 35 - 36 presently on file.

REMARKS

The Applicant notes that claims 1 and 23 have been amended, replacing the wording "time-varying" with "varying irregularly over time". The basis for this wording is found in the specification, particularly at lines 9 - 18 of page 8. Claim 5 has also been amended and a new claim inserted between claims 29 and 30 (the new claim 30). The amended claim 5 has basis in each of Figures 6 through 11 and their corresponding descriptions. The new claim 30 also has basis in Figures 6 through 11 but more particularly in Figures 4a and 4b, and in the description on page 10, line 8 through page 11, line 22. Other small amendments have also been made to other claims.

A compare document identifying the amendments made to the claims, has been attached, deleted text being struck-through and new text being underlined. No new matter has been added by way of these amendments.

Under item V. 2. of the Written Opinion, the Examiner rejected claim 1 as lacking novelty in view of the publication of patent application WO 96 01006 (the "Honeywell application"). The Applicant submits that the amended claim 1 is novel in view of the Honeywell application as the Honeywell application does not recite all of the relevant limitations of this claim. Before considering the limitations of claim 1, a review of the Honeywell application is necessary.

Firstly, it is important to understand the purpose of the Honeywell design - to reject "spurious" signals. The term "spurious" appears in the Abstract, each of the 21 claims, and repeatedly in the specification.. "Spurious" signals are defined by Honeywell on page 1 at lines 26 - 32, and again on page 6 at lines 17 - 26 with respect to a specific example: when a 90MHz LO signal is used to demodulate a desired 80MHz signal, and there is a 100MHz "spurious" signal in the signal path, then both the desired signal and the spurious signal will demodulate to 10MHz. They explain that it is generally impossible to separate these two signals as they will overlap one another at 10MHz.

Honeywell proposes a two-stage mixing topology that demodulates the desired signal, but suppresses this spurious signal. They do this by using two local oscillators (LO) that one would see in a typical superheterodyne topology, except that the two LO signals are modulated with the same spread spectrum (SS) pattern before they mix with the input signal.

They argue that the desired 80MHz signal will be encoded by the first SS LO, and then decoded by the second. They also argue that the 100MHz will not be properly decoded by the second SS LO, so this signal would simply remain as noise at the output (lines 20 - 21 of page 6 read: "In other words, the desired signal is correctly spread in the bandwidth but the undesired signal is not." At lines 25 - 26 of page 6, Honeywell then notes: "... the desired signal may be recovered since it is spread differently from the undesired signal.")

Honeywell does not explain how or why this works, but they clearly argue that this topology will not modulate or demodulate all input signals - only the desired input signal. Note that the filter plays no part in this selection process, as in the example they present, the intermediate frequency (IF) of both the 80MHz and 100MHz inputs will be the same - 10MHz.

Looking now at the amended claim 1, we see the limitation at lines 7 - 8 that "φ_1 * φ_2 has significant power at the frequency of a local oscillator signal being emulated", and at lines 10 - 11 that the second mixer will "generate an output signal $x(t)$ φ_1 φ_2". Clearly, Honeywell is arguing that their modulation/demodulation topology does not

satisfy either of these requirements, otherwise both the 80MHz and 100MHz signals would be demodulated equally, down to 1MHz at the output. That is:

- the claim requires the output to be equal to $x(t)\ \varphi_1\ \varphi_2$;
- given inputs of 80MHz and 100MHz, and SS LO signals of 90MHz of 9MHz, what is the output of the Honeywell topology?
- according to the Honeywell document, the 80MHz will be demodulated to 1MHz, but the 100MHz signal will not;
- however, if the output of the Honeywell topology was equal to $x(t)\ \varphi_1\ \varphi_2$, then it would demodulate both the 80MHz and 100MHz signals down to 1MHz, overlapping one another;
- it does not, thus, the Honeywell application does not anticipate the limitations of claim 1

Therefore, claim 1 is in compliance with the requirements of PCT Article 33(1), (2).

The Applicant also notes that because Honeywell is attempting to address a different problem than that of the invention (i.e. rejecting spurious input signals), that the skilled technician would not consider the Honeywell application in addressing the problems of the invention.

Also under item V. 2., the Examiner submitted that a typical superheterodyne topology also anticipates claim 1, as any LO signal produces a "time-varying" signal. While the Applicant feels that the meaning of the term "time-varying" is clear from a reading of the patent specification as a whole, he has amended this wording to "which varies irregularly over time", to make the distinction more clear. As noted above, this wording has basis in the specification at lines 9 - 18 of page 8.

The Applicant therefore asks that the Examiner withdraw this objection under PCT Article 33(1), (2).

Under item V. 3., the Examiner submitted that the balance of the claims lack an inventive step in view of various prior references. The Applicant notes that all of these claims incorporate the limitations of claim 1. As presented above, claim 1 is novel and non-obvious in view of the cited references, therefore, the Applicant submits that each claim reciting at least the same limitations would similarly be novel and non-obvious.

Therefore, the Application asks that the Examiner withdraw this objection under PCT Article 56.

With regard to item VII. 1., Applicant submits that the inclusion of reference numbers in the claims is not entirely appropriate as the figures do not correspond precisely with the elements of the claims. The Applicant submits that it would be confusing to make reference to the figures as requested.

With regard to item VII. 2., Applicant wishes to defer the amendment of the Background to the Invention until national entry applications have been filed.

The Applicant submits that he has complied with the requirements of item VII. 3., noting that the basis for the amendments to the claims is provided above.

With regard to item VIII. 1., the Applicant disagrees with the Examiner, submitting that the scope of claim 1 would be clear to one skilled in the art. As noted in Article 6, II-4.2 of the PCT Guidelines: "The claim should also be read with an attempt to make technical sense out of it".

With regard to item VIII. 2., the Applicant again disagrees with the Examiner, as the scope of claim 2 would also be clear to one skilled in the art. While an input signal $x(t)$ may include spurious signals, noise, etc., it would be clear to the reader that an up-convertor would be designed with a particular purpose in mind, and that part of this design process would be the specification of the input and output signals involved.

The Applicant therefore asks that the Examiner withdraw these objections under PCT Article 6.

The Applicant believes that all of the objections levelled by the Examiner have now been addressed. The Applicant would be pleased to discuss any outstanding or new issues which may arise during preparation of a second Written Opinion, or the International Preliminary Examination Report.

for T. Gary O'Neill
Agent for the Applicant
TGO:MKL

117612.1

COMPARE DOCUMENT

WHAT IS CLAIMED IS:

1. A synthesizer for generating signals to be input to successive mixers for modulating or demodulating an input signal *x(t)*, said synthesizer comprising:

a first signal generator for producing a first ~~time-varying~~mixing signal φ_1 which varies irregularly over time; and

a second signal generator for producing a second ~~time-varying~~mixing signal φ_2 which varies irregularly over time;

where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated.

2. The synthesizer of claim 1, wherein signals used to generate φ_1 and φ_2 do not have a significant amount of power at the output frequency of said output signal $x(t)$ φ_1 φ_2.

3. The synthesizer of claim 2, wherein $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)$ φ_1 φ_2.

4. The synthesizer of claim 3, wherein $\varphi_2 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)$ φ_1 φ_2.

5. The synthesizer of claim 4, wherein said first and second ~~time-varying~~mixing signals φ_1 and φ_2 are ~~irregular~~generating using a single time base.

6. The synthesizer of claim 4, wherein said first and second ~~time-varying~~mixing signals φ_1 and φ_2 are digital waveforms.

7. The synthesizer of claim 4, wherein said first and second ~~time-varying~~mixing signals φ_1 and φ_2 are square waveforms.

8. The synthesizer of claim 4, wherein said first and second ~~time-varying~~mixing signals φ_1 and φ_2 are randomly generated.

9. The synthesizer of claim 4, wherein said first and second ~~time-varying~~mixing signals φ_1 and φ_2 are pseudo-randomly generated.

10. The synthesizer of claim 4, wherein said first and second ~~time-varying~~mixing signals φ_1 and φ_2 are periodic functions of time.

11. The synthesizer of claim 4, wherein said first and second signal generators comprise:

pulse removal means for removing pulses from a local oscillator signal which has a frequency of twice the RF carrier, generating said first ~~time-varying~~mixing signal φ_1; and

complementary means for generating said second ~~time-varying~~mixing signal φ_2.

12. The synthesizer of claim 4, wherein said pulse removal means comprises:

a pulse swallower for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and swallowing each pulse with a control signal *S*; and

a divide by two circuit for receiving and dividing said pulse swallowed signal by two, producing said first ~~time-varying~~mixing signal φ_1.

13. The synthesizer of claim 12, wherein said complementary means comprises:

a delay circuit for receiving and delaying said control signal *S* to be synchronized in time with said first ~~time-varying~~mixing signal φ_1, outputting said delayed control signal *S* as said second ~~time-varying~~mixing signal φ_2.

14. The synthesizer of claim 4, wherein said first and second signal generators comprise:

shift register means for generating said first and second ~~time-varying~~mixing signals φ_1 and φ_2 by shifting out corresponding predetermined sequences.

15. The synthesizer of claim 14, wherein said shift register means comprises:

a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first ~~time-varying~~mixing signal φ_1, by shifting out a predetermined sequence.

16. The synthesizer of claim 15, wherein said second signal generator comprises:

an exclusive-OR (XOR) circuit for comparing outputs of consecutive latches in said shift register; and

a second shift register being clocked by said XOR output, and generating said second ~~time-varying~~mixing signal φ_2, by shifting out a second predetermined sequence.

17. The synthesizer of claim 15, wherein said second signal generator comprises:

a third shift register for receiving said oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said second ~~time-varying~~mixing signal φ_2, by shifting out a predetermined sequence.

18. The synthesizer of claim 4, wherein said first and second signal generators comprise:

means for generating said first ~~time-varying~~mixing signal φ_1 from an oscillator signal at the frequency of the local oscillator signal being emulated, and a control signal *S* having edges aligned with said oscillator signal; and

means for delaying said control signal *S* to produce said second ~~time-varying~~mixing signal φ_2.

19. The synthesizer of claim 18, wherein said means for delaying comprises:

a delay latch for sampling said control signal *S* at the frequency of the local oscillator signal being emulated; and

an invertor for receiving and inverting said delay latched control signal *S* to produce said second ~~time-varying~~mixing signal φ_2.

20. The synthesizer of claim 19, wherein said means for generating said first ~~time-varying~~mixing signal φ_1 comprises:

a second invertor for receiving the oscillator signal at the frequency of the local oscillator signal being emulated; and

an exclusive-OR (XOR) circuit for comparing said inverted oscillator signal with said latched input signal *x(t)*, producing said first ~~time-varying~~mixing signal φ_1.

21. The synthesizer of claim 4, wherein said first signal generator comprises:

a shift register with a feedback loop.

22. The synthesizer of claim 21, wherein said first signal generator comprises:

a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first ~~time-varying~~mixing signal φ_1, by shifting out a predetermined sequence; and

a modulo-2 multiplier for receiving said first ~~time-varying~~mixing signal φ_1 and the output of an earlier latch in said shift register, feeding an output into a later latch in said shift register.

23. The synthesizer of claim 4 comprising:

one or more additional signal generators for producing one or more additional ~~time-varying~~mixing signals, varying irregularly over time;

where the product of all of said ~~time-varying~~mixing signals has significant power at the frequency of a local oscillator signal being emulated, and none of said all of said ~~time-varying~~mixing signals has significant power at the frequency of said local oscillator signal being emulated.

24. The synthesizer of claim 4, where said first signal generator comprises:

a divide by 2 circuit for receiving an oscillator signal at the frequency of the local oscillator signal being emulated; and

a divide by 4 circuit for receiving said oscillator signal at the frequency of the local oscillator signal being emulated;

selector means for routing either the output of said divide by 2 circuit or said divide by 4 circuit to an output, said output producing said first ~~time-varying~~mixing signal φ_1.

25. The synthesizer of any one of claims 12, 13, 18, 19 or 2~~4~~0, wherein said control signal S comprises a random signal.

26. The synthesizer of any one of claims 12, 13, 18, 19 or 2~~4~~0, wherein said control signal S comprises a pseudo-random signal.

27. The synthesizer of any one of claims 12, 13, 18, 19 or 2~~4~~0, wherein said control signal S comprises a periodic signal.

28. The synthesizer of any one of claims 12, 13, 18, 19 or 2~~4~~0, comprising:

a delta-sigma (~~i.e.~~ Δ-S) modulator for generating said control signal *S*.

29. The synthesizer of claim 4 comprising:
first and second latches which are clocked via a common clock, to align said first and second ~~time-varying~~mixing signals φ_1 and φ_2.

30. The synthesizer of claim 4, wherein the patterns of said first and second mixing signals φ_1 and φ_2 are different from one another.

3~~0~~1. An integrated circuit comprising the synthesizer of any one of claims 1 - ~~29~~30.

3~~1~~2. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the synthesizer of any one of claims 1 - ~~29~~30.

3~~2~~3. A computer data signal embodied in a output wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio transmitter of any one of claims 1 - ~~29~~30.

NEW CLAIMS

WHAT IS CLAIMED IS:

1. A synthesizer for generating signals to be input to successive mixers for modulating or demodulating an input signal *x(t)*, said synthesizer comprising:

a first signal generator for producing a first mixing signal φ_1 which varies irregularly over time; and

a second signal generator for producing a second mixing signal φ_2 which varies irregularly over time;

where $\varphi_1 * \varphi_2$ has significant power at the frequency of a local oscillator signal being emulated, and neither φ_1 nor φ_2 has significant power at the frequency of said local oscillator signal being emulated.

2. The synthesizer of claim 1, wherein signals used to generate φ_1 and φ_2 do not have a significant amount of power at the output frequency of said output signal $x(t)\ \varphi_1\ \varphi_2$.

3. The synthesizer of claim 2, wherein $\varphi_1 * \varphi_1 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)\ \varphi_1\ \varphi_2$.

4. The synthesizer of claim 3, wherein $\varphi_2 * \varphi_2$ does not have a significant amount of power within the bandwidth of said output signal $x(t)\ \varphi_1\ \varphi_2$.

5. The synthesizer of claim 4, wherein said first and second mixing signals φ_1 and φ_2 are generating using a single time base.

6. The synthesizer of claim 4, wherein said first and second mixing signals φ_1 and φ_2 are digital waveforms.

7. The synthesizer of claim 4, wherein said first and second mixing signals φ_1 and φ_2 are square waveforms.

8. The synthesizer of claim 4, wherein said first and second mixing signals φ_1 and φ_2 are randomly generated.

9. The synthesizer of claim 4, wherein said first and second mixing signals φ_1 and φ_2 are pseudo-randomly generated.

10. The synthesizer of claim 4, wherein said first and second mixing signals φ_1 and φ_2 are periodic functions of time.

11. The synthesizer of claim 4, wherein said first and second signal generators comprise:

pulse removal means for removing pulses from a local oscillator signal which has a frequency of twice the RF carrier, generating said first mixing signal φ_1; and

complementary means for generating said second mixing signal φ_2.

12. The synthesizer of claim 4, wherein said pulse removal means comprises:

a pulse swallower for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and swallowing each pulse with a control signal *S*; and

a divide by two circuit for receiving and dividing said pulse swallowed signal by two, producing said first mixing signal φ_1.

13. The synthesizer of claim 12, wherein said complementary means comprises:

a delay circuit for receiving and delaying said control signal *S* to be synchronized in time with said first mixing signal φ_1, outputting said delayed control signal *S* as said second mixing signal φ_2.

14. The synthesizer of claim 4, wherein said first and second signal generators comprise:

shift register means for generating said first and second mixing signals φ_1 and φ_2 by shifting out corresponding predetermined sequences.

15. The synthesizer of claim 14, wherein said shift register means comprises:

a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first mixing signal φ_1, by shifting out a predetermined sequence.

16. The synthesizer of claim 15, wherein said second signal generator comprises:

an exclusive-OR (XOR) circuit for comparing outputs of consecutive latches in said shift register; and

a second shift register being clocked by said XOR output, and generating said second mixing signal φ_2, by shifting out a second predetermined sequence.

17. The synthesizer of claim 15, wherein said second signal generator comprises:

a third shift register for receiving said oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said second mixing signal φ_2, by shifting out a predetermined sequence.

18. The synthesizer of claim 4, wherein said first and second signal generators comprise:

means for generating said first mixing signal φ_1 from an oscillator signal at the frequency of the local oscillator signal being emulated, and a control signal *S* having edges aligned with said oscillator signal; and

means for delaying said control signal *S* to produce said second mixing signal φ_2.

19. The synthesizer of claim 18, wherein said means for delaying comprises:

a delay latch for sampling said control signal *S* at the frequency of the local oscillator signal being emulated; and

an invertor for receiving and inverting said delay latched control signal *S* to produce said second mixing signal φ_2.

20. The synthesizer of claim 19, wherein said means for generating said first mixing signal φ_1 comprises:

a second invertor for receiving the oscillator signal at the frequency of the local oscillator signal being emulated; and

an exclusive-OR (XOR) circuit for comparing said inverted oscillator signal with said latched input signal *x(t)*, producing said first mixing signal φ_1.

21. The synthesizer of claim 4, wherein said first signal generator comprises:

a shift register with a feedback loop.

22. The synthesizer of claim 21, wherein said first signal generator comprises:

a shift register for receiving an oscillator signal at twice the frequency of the local oscillator signal being emulated, and generating said first mixing signal φ_1, by shifting out a predetermined sequence; and

a modulo-2 multiplier for receiving said first mixing signal φ_1 and the output of an earlier latch in said shift register, feeding an output into a later latch in said shift register.

23. The synthesizer of claim 4 comprising:

one or more additional signal generators for producing one or more additional mixing signals, varying irregularly over time;

where the product of all of said mixing signals has significant power at the frequency of a local oscillator signal being emulated, and none of said all of said mixing signals has significant power at the frequency of said local oscillator signal being emulated.

24. The synthesizer of claim 4, where said first signal generator comprises:

a divide by 2 circuit for receiving an oscillator signal at the frequency of the local oscillator signal being emulated; and

a divide by 4 circuit for receiving said oscillator signal at the frequency of the local oscillator signal being emulated;

selector means for routing either the output of said divide by 2 circuit or said divide by 4 circuit to an output, said output producing said first mixing signal φ_1.

25. The synthesizer of any one of claims 12, 13, 18, 19 or 20, wherein said control signal S comprises a random signal.

26. The synthesizer of any one of claims 12, 13, 18, 19 or 20, wherein said control signal S comprises a pseudo-random signal.

27. The synthesizer of any one of claims 12, 13, 18, 19 or 20, wherein said control signal S comprises a periodic signal.

28. The synthesizer of any one of claims 12, 13, 18, 19 or 20, comprising:

a delta-sigma (Δ-S) modulator for generating said control signal *S*.

29. The synthesizer of claim 4 comprising:

first and second latches which are clocked via a common clock, to align said first and second mixing signals φ_1 and φ_2.

30. The synthesizer of claim 4, wherein the patterns of said first and second mixing signals φ_1 and φ_2 are different from one another.

31. An integrated circuit comprising the synthesizer of any one of claims 1 - 30.

32. A computer readable memory medium, storing computer software code in a hardware development language for fabrication of an integrated circuit comprising the synthesizer of any one of claims 1 - 30.

33. A computer data signal embodied in a output wave, said computer data signal comprising computer software code in a hardware development language for fabrication of an integrated circuit comprising the radio transmitter of any one of claims 1 - 30.

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT OR THE DECLARATION

(PCT Rule 44.1)

To:
Gowling Lafleur Henderson LLP
Attn. Wada, Ikuku
Suite 2600
160 Elgin Street
Ottawa, Ontario K1P 1C3
CANADA

Applicant's or agent's file reference 08-891710WO	Date of mailing *(day/month/year)* 25/10/2002
International application No. PCT/CA 01/ 00876	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
Applicant SIRIFIC WIRELESS CORPORATION et al.	International filing date *(day/month/year)* 19/06/2001

1. [X] The applicant is hereby notified that the International Search Report has been established and is transmitted herewith.

Filing of amendments and statement under Article 19:
The applicant is entitled, if he so wishes, to amend the claims of the International Application (see Rule 46):

When? The time limit for filing such amendments is normally 2 months from the date of transmittal of the International Search Report; however, for more details, see the notes on the accompanying sheet.

Where? Directly to the International Bureau of WIPO
34, chemin des Colombettes
1211 Geneva 20, Switzerland
Fascimile No.: (41-22) 740.14.35

For more detailed instructions, see the notes on the accompanying sheet.

2. [ ] The applicant is hereby notified that no International Search Report will be established and that the declaration under Article 17(2)(a) to that effect is transmitted herewith.

3. [ ] **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

[ ] the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

[ ] no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Further action(s):** The applicant is reminded of the following:

Shortly after **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

Within **19 months** from the priority date, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase until 30 months from the priority date (in some Offices even later).

Within **20 months** from the priority date, the applicant must perform the prescribed acts for entry into the national phase before all designated Offices which have not been elected in the demand or in a later election within 19 months from the priority date or could not be elected because they are not bound by Chapter II.

Name and mailing address of the International Searching Authority European Patent Office, P.B. 5818 Patentlaan 2 NL-2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Authorized officer Mareike Zambuto

Form PCT/ISA/220 (July 1998)

NOTES TO FORM PCT/ISA/220

These Notes are intended to give the basic instructions concerning the filing of amendments under article 19. The Notes are based on the requirements of the Patent Cooperation Treaty, the Regulations and the Administrative Instructions under that Treaty. In case of discrepancy between these Notes and those requirements, the latter are applicable. For more detailed information, see also the PCT Applicant's Guide, a publication of WIPO.

In these Notes, "Article", "Rule", and "Section" refer to the provisions of the PCT, the PCT Regulations and the PCT Administrative Instructions respectively.

INSTRUCTIONS CONCERNING AMENDMENTS UNDER ARTICLE 19

The applicant has, after having received the international search report, one opportunity to amend the claims of the international application. It should however be emphasized that, since all parts of the international application (claims, description and drawings) may be amended during the international preliminary examination procedure, there is usually no need to file amendments of the claims under Article 19 except where, e.g. the applicant wants the latter to be published for the purposes of provisional protection or has another reason for amending the claims before international pbulication. Furthermore, it should be emphasized that provisional protection is available in some States only.

What parts of the international application may be amended?

Under Article 19, only the claims may be amended.

During the international phase, the claims may also be amended (or further amended) under Article 34 before the International Preliminary Examining Authority. The description and drawings may only be amended under Article 34 before the International Examining Authority.

Upon entry into the national phase, all parts of the international application may be amended under Article 28 or, where applicable, Article 41.

When? Within 2 months from the date of transmittal of the international search report or 16 months from the priority date, whichever time limit expires later. It should be noted, however, that the amendments will be considered as having been received on time if they are received by the International Bureau after the expiration of the applicable time limit but before the completion of the technical preparations for international publication (Rule 46.1).

Where not to file the amendments?

The amendments may only be filed with the International Bureau and not with the receiving Office or the International Searching Authority (Rule 46.2).

Where a demand for international preliminary examination has been/is filed, see below.

How? Either by cancelling one or more entire claims, by adding one or more new claims or by amending the text of one or more of the claims as filed.

A replacement sheet must be submitted for each sheet of the claims which, on account of an amendment or amendments, differs from the sheet originally filed.

All the claims appearing on a replacement sheet must be numbered in Arabic numerals. Where a claim is cancelled, no renumbering of the other claims is required. In all cases where claims are renumbered, they must be renumbered consecutively (Administrative Instructions, Section 205(b)).

The amendments must be made in the language in which the international application is to be published.

What documents must/may accompany the amendments?

Letter (Section 205(b)):

The amendments must be submitted with a letter.

The letter will not be published with the international application and the amended claims. It should not be confused with the "Statement under Article 19(1)" (see below, under "Statement under Article 19(1)").

The letter must be in English or French, at the choice of the applicant. However, if the language of the international application is English, the letter must be in English; if the language of the international application is French, the letter must be in French.

The letter must indicate the differences between the claims as filed and the claims as amended. It must, in particular, indicate, in connection with each claim appearing in the international application (it being understood that identical indications concerning several claims may be grouped),whether

(i) the claim is unchanged;

(ii) the claim is cancelled;

(iii) the claim is new;

(iv) the claim replaces one or more claims as filed;

(v) the claim is the result of the division of a claim as filed.

The following examples illustrate the manner in which amendments must be explained in the accompanying letter:

1. [Where originally there were 48 claims and after amendment of some claims there are 51]:
"Claims 1 to 29, 31, 32, 34, 35, 37 to 48 replaced by amended claims bearing the same numbers; claims 30, 33 and 36 unchanged; new claims 49 to 51 added."

2. [Where originally there were 15 claims and after amendment of all claims there are 11]:
"Claims 1 to 15 replaced by amended claims 1 to 11."

3. [Where originally there were 14 claims and the amendments consist in cancelling some claims and in adding new claims]:
"Claims 1 to 6 and 14 unchanged; claims 7 to 13 cancelled; new claims 15, 16 and 17 added." or
"Claims 7 to 13 cancelled; new claims 15, 16 and 17 added; all other claims unchanged."

4. [Where various kinds of amendments are made]:
"Claims 1-10 unchanged; claims 11 to 13, 18 and 19 cancelled; claims 14, 15 and 16 replaced by amended claim 14; claim 17 subdivided into amended claims 15, 16 and 17; new claims 20 and 21 added."

"Statement under article 19(1)" (Rule 46.4)

The amendments may be accompanied by a statement explaining the amendments and indicating any impact that such amendments might have on the description and the drawings (which cannot be amended under Article 19(1)).

The statement will be published with the international application and the amended claims.

It must be in the language in which the international appplication is to be published.

It must be brief, not exceeding 500 words if in English or if translated into English.

It should not be confused with and does not replace the letter indicating the differences between the claims as filed and as amended. It must be filed on a separate sheet and must be identified as such by a heading, preferably by using the words "Statement under Article 19(1)."

It may not contain any disparaging comments on the international search report or the relevance of citations contained in that report. Reference to citations, relevant to a given claim, contained in the international search report may be made only in connection with an amendment of that claim.

Consequence if a demand for international preliminary examination has already been filed

If, at the time of filing any amendments under Article 19, a demand for international preliminary examination has already been submitted, the applicant must preferably, at the same time of filing the amendments with the International Bureau, also file a copy of such amendments with the International Preliminary Examining Authority (see Rule 62.2(a), first sentence).

Consequence with regard to translation of the international application for entry into the national phase

The applicant's attention is drawn to the fact that, where upon entry into the national phase, a translation of the claims as amended under Article 19 may have to be furnished to the designated/elected Offices, instead of, or in addition to, the translation of the claims as filed.

For further details on the requirements of each designated/elected Office, see Volume II of the PCT Applicant's Guide.

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION** see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
08-891710WO		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/CA 01/ 00876	19/06/2001	01/09/2000
Applicant		
SIRIFIC WIRELESS CORPORATION et al.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 3 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language,** the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

   [ ] contained in the international application in written form.

   [ ] filed together with the international application in computer readable form.

   [ ] furnished subsequently to this Authority in written form.

   [ ] furnished subsequently to this Authority in computer readble form.

   [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 4

   [X] as suggested by the applicant.

   [ ] because the applicant failed to suggest a figure.

   [ ] because this figure better characterizes the invention.

   [ ] None of the figures.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/CA 01/00876

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04B1/04 H03D7/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04B H03D H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	GB 2 331 207 A (SAMSUNG LTD) 12 May 1999 (1999-05-12) page 1, line 11 -page 2, line 11; figures 1,2	1-7, 12-19, 27-42
Y	page 3, line 16 - line 30 page 6, line 21 -page 8, line 5; figure 3 ---	20-26
Y	US 4 110 834 A (M. ALTWEIN) 29 August 1978 (1978-08-29) column 3, line 63 -column 4, line 24; figure 1 column 8, line 17 - line 37; figure 5 --- -/--	20-26

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 October 2002	25/10/2002

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Butler, N

1

Form PCT/ISA/210 (second sheet) (July 1992)

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication,where appropriate, of the relevant passages	Relevant to claim No.
X	US 5 838 717 A (S. ISHII) 17 November 1998 (1998-11-17) column 1, line 35 -column 3, line 30; figure 7 column 5, line 38 - line 65; figure 1	1-7, 12-19, 27-42
X	EP 0 902 549 A (SAMSUNG LTD) 17 March 1999 (1999-03-17) column 1, line 10 -column 2, line 48; figures 1,2 column 5, line 8 -column 8, line 24; figures 4,5	1
X	V. AUE:. "multi-carrier spread spectrum modulation with reduced dynamic range" VEHICULAR TECHNOLOGY CONFERENCE 1996 IEEE, vol. 2, 28 April 1996 (1996-04-28), pages 914-917, XP010162522 atlanta us page 914, column 1, line 6 -page 915, column 1, line 52; figure 1	1,28
X	WO 96 01006 A (HONEYWELL INC) 11 January 1996 (1996-01-11) page 2, line 18 -page 3, line 25 page 4, line 5 -page 5, line 32; figure 2	1
X	US 5 390 346 A (D. MARZ) 14 February 1995 (1995-02-14) column 4, line 34 -column 5, line 60; figure 1	1
X	EP 0 837 565 A (LUCENT INC,) 22 April 1998 (1998-04-22) page 2, column 34, line 3 -page 5, column 2 page 6, line 15 - line 32; figure 6	1
X	EP 0 977 351 A (MOTOROLA INC,) 2 February 2000 (2000-02-02) page 4, line 33 -page 5, line 29; figure 1	1
A	US 6 014 408 A (T. NARUSE) 11 January 2000 (2000-01-11) column 1, line 14 - line 42; figures 1,2 column 6, line 32 -column 7, line 39 column 10, line 30 -column 11, line 27; figure 4	20-26

1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/CA 01/00876

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
GB 2331207 A	12-05-1999	KR 264862 B1	01-09-2000
		CN 1211861 A ,B	24-03-1999
		JP 11098120 A	09-04-1999
		SE 9802651 A	01-02-1999
US 4110834 A	29-08-1978	DE 2627586 A1	22-12-1977
		GB 1550481 A	15-08-1979
		JP 1207193 C	11-05-1984
		JP 52156531 A	27-12-1977
		JP 58039355 B	29-08-1983
US 5838717 A	17-11-1998	JP 2737655 B2	08-04-1998
		JP 8032485 A	02-02-1996
		DE 19525428 A1	18-01-1996
EP 902549 A	17-03-1999	CN 1278129 A	27-12-2000
		EP 0902549 A2	17-03-1999
		JP 3093182 B2	03-10-2000
		JP 11163827 A	18-06-1999
WO 9601006 A	11-01-1996	AU 2909795 A	25-01-1996
		WO 9601006 A1	11-01-1996
US 5390346 A	14-02-1995	NONE	
EP 837565 A	22-04-1998	US 5956345 A	21-09-1999
		CA 2212265 A1	13-03-1998
		EP 0837565 A1	22-04-1998
		JP 10107691 A	24-04-1998
		US 6256290 B1	03-07-2001
EP 977351 A	02-02-2000	EP 0977351 A1	02-02-2000
		CN 1250338 A	12-04-2000
		JP 2000106533 A	11-04-2000
US 6014408 A	11-01-2000	JP 10190527 A	21-07-1998

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference	**FOR FURTHER ACTION** see Notification of Transmittal of International Search Report (Form PCT/ISA/220) as well as, where applicable, item 5 below.	
08-887955WO		
International application No.	International filing date *(day/month/year)*	(Earliest) Priority Date *(day/month/year)*
PCT/CA 00/ 00996	01/09/2000	01/09/1999
Applicant		
SIRIFIC WIRELESS CORPORATION et al.		

This International Search Report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This International Search Report consists of a total of 2 sheets.

[X] It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language,** the international search was carried out on the basis of the international application in the language in which it was filed, unless otherwise indicated under this item.

   [ ] the international search was carried out on the basis of a translation of the international application furnished to this Authority (Rule 23.1(b)).

   b. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international search was carried out on the basis of the sequence listing :

   [ ] contained in the international application in written form.

   [ ] filed together with the international application in computer readable form.

   [ ] furnished subsequently to this Authority in written form.

   [ ] furnished subsequently to this Authority in computer readble form.

   [ ] the statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

   [ ] the statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished

2. [ ] **Certain claims were found unsearchable** (See Box I).

3. [ ] **Unity of invention is lacking** (see Box II).

4. With regard to the **title,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established by this Authority to read as follows:

5. With regard to the **abstract,**

   [X] the text is approved as submitted by the applicant.

   [ ] the text has been established, according to Rule 38.2(b), by this Authority as it appears in Box III. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. The figure of the **drawings** to be published with the abstract is Figure No. 6

   [X] as suggested by the applicant.

   [ ] because the applicant failed to suggest a figure.

   [ ] because this figure better characterizes the invention.

   [ ] None of the figures.

INTERNATIONAL SEARCH REPORT

International Application No
PCT/CA 00/00996

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04B1/26 H04B1/28 H03D7/16

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H04B H03D

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 96 01006 A (HONEYWELL INC) 11 January 1996 (1996-01-11) abstract page 2, line 1 - line 16 page 4, line 5 - line 22 claims 1-7; figure 2	1-10
X	EP 0 899 868 A (MITEL CORP) 3 March 1999 (1999-03-03) abstract column 1, line 22 - line 42 claims 1-6	1-10

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
16 January 2001	24/01/2001

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Lazaridis, P

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/CA 00/00996

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9601006 A	11-01-1996	AU 2909795 A	25-01-1996
EP 0899868 A	03-03-1999	CA 2245958 A	28-02-1999